Biographical Sketch - Eby G. Friedman

Contact Information

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Education

Ph. D. Electrical Engineering	1985-1989	University of California	Irvine, California
M. S. Electrical Engineering	1979-1981	University of California	Irvine, California
B. S. Electrical Engineering	1975-1979	Lafayette College	Easton, Pennsylvania

Professional Experience

University of Rochester, Dept of Electrical and Computer Engineering, Rochester, New York
- Distinguished Professor, 2002 to present
- Professor, 1998 to 2002
- Director, Center for Electronic Imaging Systems (CEIS), '99 to '08
  - direct center for the research and technology transfer of imaging technologies and microelectronics circuits into large and small corporate commercial applications
- Director, High Performance VLSI/IC Design and Analysis Laboratory, '91 to present
  - research and teaching in the areas of high performance VLSI/IC design and analysis with emphasis on technology issues and their system applications
- Associate Professor, 1991 to 1995, With unlimited tenure - 1995 to 1998

Technion - Israel Institute of Technology, Faculty of Electrical Engineering
- Visiting Professor, 2005 to present
- Co-Director, Advanced Circuits Research Center (ACRC) - 2011 to present
- Member, Board of Governors - 2017 to present

Hughes Aircraft Company, Technology Center, Carlsbad, California
- Department Manager, 1988-1991
- Section Head, 1984-1988
- Technical Supervisor, 1983-1984
  - designed specialized high performance VHSIC and VLSI integrated circuits
  - principal investigator developing applied R & D in high performance circuit design techniques and methodologies
  - managed design and test organization responsible for developing high performance digital and analog CMOS and BIMOS integrated circuits from behavioral specification to pattern generation and functional/parametric test

Hughes Aircraft Company, LSI Center, Newport Beach, California
Project Engineer, 1982-1983
Member of Technical Staff, 1979-1982
designed and managed product oriented integrated circuits used in a variety of applications

N. V. Philips Gloeilampen Fabrieken, Eindhoven, The Netherlands
Engineer-in-Training, 1978
research performed on experimental differential amplifier circuit used in the restoration of color television signals

Honors and Awards

IEEE Circuits and Systems Mac Van Valkenburg Award 2018
"For technical leadership in high performance integrated circuit design"
Member, Board of Governors, Technion - Institute of Technology 2017
University of California, Irvine Engineering Hall of Fame 2016
IEEE Circuits and Systems Society Guillemin-Cauer Best Paper Award 2015
Hilda and Hershel Rich Technion Innovation Award 2014
IEEE Circuits and Systems Charles A. Desoer Technical Achievement Award 2013
"For technical leadership in circuit and interconnect design techniques and methodologies in clock, power, and signal delivery for two- and three-dimensional integrated systems"
Sanford Kaplan Prize for Creative Management in High Tech in the 21st Century 2013
IEEE Circuits and Systems Society VLSI Transactions Best Paper Award 2012
Recognition of Service Award in Appreciation for Contributions to ACM 2007
GRC Inventor Recognition Award 2007
Technology Transfer Award for Outstanding New York State Economic Impact 2006
William H. Riker University Award for Excellence in Graduate Teaching 2005
Best Paper Award for IEEE/ACM Great Lakes Symposium on VLSI 2005
IEEE CAS Achievement Award 2004
Best Paper Finalist - IEEE Int. Conference on Electronics, Circuits and Systems 2004
Fulbright Scholar 2000-2001
Distinguished Lecturer of the IEEE CAS Society 2000-2001
IEEE Fellow 2000
"For contributions to high performance circuit design and VLSI-based synchronous systems."
IBM University Research Award 1997
Outstanding Chapter Chairman for IEEE Rochester section 1996
University of Rochester Engineering College Teaching Excellence Award 1994
DoD Augmentation Award for Science and Engineering Research Training 1993
NSF Research Initiation Award 1992
Senior Member of IEEE 1990
Howard Hughes Doctoral Fellowship 1986-1989
(1st Doctoral Fellow "Department Manager" in history of Hughes Aircraft Company)
Howard Hughes Masters Fellowship 1980-1981

Professional Activities and Service

Journals and Transactions

Editor-in-Chief	*Microelectronics Journal* - '14 to present
	IEEE Transactions on Very Large Scale Integration (VLSI) Systems - '01 to '02
Regional Editor	*Journal of Circuits, Systems, and Computers* (US Regional Editor) - '99 to '13
Associate Editor	*IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* - '93 to '95 (Topic area: Digital VLSI Circuits and Signal Processing)
	Analog Integrated Circuits and Signal Processing - '95 to present
	IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing - '99 to '01 (Topic area: VLSI Digital Circuits and Signal Processing)
	Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology / Signal Processing Systems- '01 to 2015
	Proceedings of the IEEE - 2002 to 2004
	Microelectronics Journal - 2004 to 2014
	Journal of Low Power Electronics - 2004 to present
	Journal of Low Power Electronics and Applications - 2010 to present
	IEEE Journal on Emerging and Selected Topics in Circuits and Systems - 2011 to 2015

Professional Society Committees and Associations

Officer	The VLSI Systems and Applications Technical Committee (VSATC) of the IEEE Circuits and Systems Society (Secretary, '93-'94, Chair, '95-'96)
	IEEE Rochester Section, Electron Device Society Chapter (Treasurer, '92-'93, Secretary, '93-'94, Vice-Chair, '94-'95, Chair, '95-'96)
	IEEE Circuits and Systems Society Liaison to Solid-State Circuits Society -'97-'00
	IEEE Circuits and Systems Darlington and Guillemin-Cauer Awards (Chair, '97)
	IEEE Circuits and Systems Board of Governors (CAS BoG) - '98 - '04
	IEEE Circuits and Systems Publications Steering Committee - '98, '99, '00
	CAS Industrial Pioneer Award Committee (Chair, '01)
	CAS Society IEEE Fellow Committee (Chair, '06). Member, '07, '12
	CAS Society Van Valkenburg Award Committee (Chair, '12)

Publications and Presentations

Authored Books

1. V. F. Pavlidis, I. Savidis, and E. G. Friedman, *Three-Dimensional Integrated Circuit Design, 2nd Edition*, Morgan Kaufmann, 2017, ISBN # 978-0124105010.

2. I. P. Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Köse, and E. G. Friedman, *On-Chip Power Delivery and Management, 4th Edition*, Springer, 2016, ISBN-13: 978-3319293936 ISBN-10: 3319293931.

3. E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*, 716 pp., McGraw-

Hill Publishers, 2012, ISBN-10: 0071635769, ISBN-13: 978-0071635769. Chinese translation by Publishing House of Electronics Industry, 2015, Chinese ISBN # 978-7-121-25090-3.

4. J. Rosenfeld and E. G. Friedman, *On-Chip Resonance in Nanoscale Integrated Circuits: Design and Analysis Methodologies for Advanced Data, Clock, and Power Generation Networks*, Lambert Academic Publishing, 2012, ISBN 978-3659259463.

5. R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Kose, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors, Second Edition*, 618 pp., Springer, 2011, ISBN # 978-1-4419-7870-7. Chinese translation by China Machine Press, 2014, Chinese ISBN # 978-7-111-44929-4.

6. D. Velenis and E. G. Friedman, *Delay Uncertainty in High Performance Clock Distribution Networks Issues and Solutions*, Lambert Academic Publishing, 2009, ISBN 978-3-8383-2715-0.

7. M. El-Moursy and E. Friedman, *On-Chip Inductive Interconnect Design Methodologies*, VDM Verlag Dr. Muller Aktiengesellschaft & Company, 2009, ISBN 978-3-639-15724-6.

8. I. S. Kourtev, B. Taskin, and E. G. Friedman, *Timing Optimization Through Clock Skew Scheduling*, Second Edition, 265 pp., Springer Science+Business Media, 2009, ISBN # 978-0-387-71055-6.

9. V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*, Morgan Kaufmann, 2009, ISBN # 978-0-12-374343-5. Chinese translation by China Machine Press, 2013, Chinese ISBN # 978-7-111-43351-4.

10. M. Popovich, A. Mezhiba and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors*, 515 pp., Springer Verlag, 2008, ISBN # 978-0-387-71600-8.

11. V. Kursun and E. G. Friedman, *Multi-Voltage CMOS Circuit Design*, 225 pp., West Sussex, England:John Wiley & Sons Press, 2006, ISBN # 0-470-01023-1. Chinese translation by China Machine Press, 2008, Chinese ISBN # 978-7-111-23864-5.

12. A. V. Mezhiba and E. G. Friedman, *Power Distribution Networks in High Speed Integrated Circuits*, 280 pp., Norwell, Massachusetts:Kluwer Academic Publishers, 2004, ISBN # 1-4020-7534-0.

13. Y. I. Ismail and E. G. Friedman, *On-Chip Inductance in High Speed Integrated Circuits*, 303 pp., Norwell, Massachusetts:Kluwer Academic Publishers, 2001, ISBN # 0-7923-7293-X.

14. I. S. Kourtev and E. G. Friedman, *Timing Optimization Through Clock Skew Scheduling*, 194 pp., Norwell, Massachusetts:Kluwer Academic Publishers, 2000, ISBN # 0-7923-7796-6.

Edited Books

1. M. A. Bayoumi and E. G. Friedman (Eds.), *Proceedings of the 2000 IEEE Workshop on Signal Processing Systems Design and Implementation*, 839 pp., IEEE Press, 2000, ISBN # 0-7803-6488-0.

2. J. J. Becerra and E. G. Friedman (Eds.), *Analog Design Issues in Digital VLSI Circuits and Systems*, 157 pp., Norwell, Massachusetts:Kluwer Academic Publishers, 1997, ISBN # 0-7923-9950-1.

3. E. G. Friedman (Ed.), *High Performance Clock Distribution Networks*, 164 pp., Norwell,

Massachusetts:Kluwer Academic Publishers, 1997, ISBN # 0-7923-9967-6.

4. E. G. Friedman (Ed.), *Clock Distribution Networks in VLSI Circuits and Systems*, 525 pp., Piscataway, New Jersey:IEEE Press, 1995, ISBN # 978-1-4419-7618-5.

Book Chapters

1. B. Vaisband and E. G. Friedman, "TSV-to-Substrate Noise Coupling in 3D Systems," *Noise Coupling in System-on-Chip*, T. Noulis, CRC Press, Chapter 3, pp. 45 - 61, 2018, ISBN # 978-1-4987-9677-4.

2. B. Vaisband and E. G. Friedman, " 3D IC Floorplanning Based on Thermal Interactions," *Noise Coupling in System-on-Chip*, T. Noulis, CRC Press, Chapter 11, pp. 325 - 341, 2018, ISBN # 978-1-4987-9677-4.

3. I. Vaisband and E. G. Friedman, "Secure Power Management and Delivery Within Intelligent Power Networks On-Chip," *Green Photonics and Electronics*, G. Eisenstein and D. Bimberg (Eds.), Springer, pp. 173 - 201, 2017, ISBN # 978-3-319-67001-0.

4. V. F. Pavlidis and E. G. Friedman, "Physical Analysis of NoC Topologies for 3-D Integrated Systems," *3D Integration for NoC-based SoC Architectures*, A. Sheibanyrad, F. Petrot, and A. Jantsch, (Eds.), Springer, pp. 89 - 114, 2011, ISBN # 978-1-4419-7617-8.

5. V. F. Pavlidis and E. G. Friedman, "Physical Design Issues in 3-D Integrated Technologies," *VLSI-SoC: Design Methodologies for SoC and SiP,* C. Piguet, R. Reis, and D. Soudris, (Eds.), Springer, pp. 1 - 21, 2010, ISBN # 978-3-642-12266-8.

6. I. Savidis and E. G. Friedman, "Physical Design Trends for Interconnects," *On-Chip Communication Architectures System on Chip Interconnect*, S. Pasricha and N. Dutt, Morgan Kaufmann Publishers, Elsevier, Chapter 11, pp. 403 - 437, 2008, ISBN # 978-0-12-373892-9.

7. N. Nelson, G. Briggs, M. Haurylau, G. Chen, H. Chen, E. G. Friedman, P. M. Fauchet, and D. H. Albonesi, "Alleviating Thermal Constraints while Maintaining Performance via Silicon-Based On-Chip Optical Interconnects," *Unique Chips and Systems*, E. John and J. Rubio (Eds.), CRC Press, Taylor & Francis Group, LLC, Chapter 14, pp. 339 - 355, 2008, ISBN # 978-1-4200-5174-2.

8. I. S. Kourtev, B. Taskin, and E. G. Friedman, "System Timing," *The VLSI Handbook*, Second Edition, W. K. Chen (Ed.), Boca Raton, Florida:CRC Press, Taylor & Francis Group, LLC, Chapter 50, pp. 50-3 - 50-43, 2007, ISBN # 0-8493-4199-X.

9. I. S. Kourtev and E. G. Friedman, "Clock Skew Scheduling for Improved Reliability," *The Electrical Engineering Handbook*, W.-K. Chen (Editor-in-Chief), Elsevier Academic Press, Chapter III.4, pp. 231-262, 2005, ISBN # 0-12-170960-4.

10. M. A. El-Moursy and E. G. Friedman, "Design Methodologies for On-Chip Inductive Interconnect," *Interconnect-Centric Design for Advanced SoC and NoC*, J. Nurmi, H. Tenhunen, J. Isoaho, and A. Jantsch (Eds.), Norwell, Massachusetts:Kluwer Academic Publishers, Chapter 4, pp. 85-124, 2004, ISBN # 1-4020-7835-8.

11. M. A. El-Moursy and E. G. Friedman, "Optimizing Inductive Interconnect for Low Power," *System-on-Chip for Real-Time Applications*, W. Badawy and G. A. Jullien (Eds.), Norwell, Massachusetts:Kluwer Academic Publishers, Section 9.2, pp. 380-391, 2003, ISBN # 1-4020-7254-6.

12. A. V. Mezhiba and E. G. Friedman, "Trade-offs in CMOS VLSI Circuits," *Trade-offs in Analog Circuit Design The Designer's Companion*, C. Toumazou, G. Moschytz, and B. Gilbert (Eds.), Dordrecht, The Netherlands:Kluwer Academic Publishers, Chapter 3, pp. 75-114, 2002, ISBN # 1-4020-7037-3.

13. I. S. Kourtev and E. G. Friedman, "System Timing," *The VLSI Handbook*, W. K. Chen (Ed.), Boca Raton, Florida:IEEE Press/CRC Press LLC, Chapter 47, pp. 47-1 - 47-32, 1999, ISBN # 0-8493-8593-8 and *Memory, Microprocessors, and ASIC*, Boca Raton, Florida:CRC Press, Chapter 1, pp. 1-1 - 1-31, 2003, ISBN # 0-8493-1737-1.

14. E. G. Friedman, "Introduction Clock Distribution Networks in VLSI Circuits and Systems," *Clock Distribution Networks in VLSI Circuits and Systems,* E. G. Friedman (Ed.), New Jersey:IEEE Press, pp. 1-36, 1995, ISBN # 0-7803-1058-6. Also published in *High-Performance System Design*, V. G. Oklobdzija (Ed.), New Jersey:IEEE Press, pp. 270-305, 1999, ISBN # 0-7803-4716-1.

15. E. G. Friedman and J. H. Mulligan, Jr., "Pipelining and Clocking of High Performance Synchronous Digital Systems," *VLSI Signal Processing Technology,* M. A. Bayoumi and E. E. Swartzlander, Jr. (Eds.), Norwell, Massachusetts:Kluwer Academic Publishers, Chapter 4, pp. 97-133, 1994, ISBN 0-7923-9490-9.

Refereed Journal Papers

0. B. Vaisband and E. G. Friedman, " Heterogeneous 3-D ICs as a Platform for Hybrid Energy Harvesting in IoT Systems," *Future Generation Computer Systems,* Vol. 87, pp. 152 - 158, 2018.

1. B. Vaisband, A. Maurice, C. W. Tan, B. K. Tay, and E. G. Friedman, "Electrical and Thermal Models of CNT TSV and Graphite Interface," *IEEE Transactions on Electron Devices,* Volume 65, Issue 5, pp. 1880 - 1886, May 2018.

2. A. Ciprut, E. G. Friedman, "Energy-Efficient Write Scheme for Nonvolatile Resistive Crossbar Arrays with Selectors," *IEEE Transactions on Very Large Scale Integration Systems,* Vol. 26, No. 4, pp. 711 - 719, April 2018.

3. K. Xu, R. Patel, P. Raghavan, and E. G. Friedman, "Exploratory Design of On-Chip Power Delivery for 14, 10, and 7 nm and Beyond FinFET ICs," *Integration, The VLSI Journal*, Volume 61, pp. 11 - 19, 2018.

4. Y. Zhang, X. Wang, E. G. Friedman, "Memristor-Based Circuit Design for Multilayer Neural Networks," *IEEE Transactions on Circuits and Systems I: Regular Papers,* Volume 65, Number 2, pp. 677 - 686, February 2018.

5. G. Krylov and E. G. Friedman, "Design for Testability of SFQ Circuits," *IEEE Transactions on*

Applied Superconductivity, Vol. 27, Issue 8, pp. 1051 - 1057 (1302307), December 2017.

6. A. Shapiro and E. G. Friedman, "Interconnect Delay Model for Wide Supply Voltage Range Repeater Insertion in Sub-22 nm FinFET Technologies," *Journal of Low Power Electronics,* Vol. 13, No. 3, pp. 395 - 401, September 2017.

7. Y. Zhang, L.Yi, X. Wang, and E. G. Friedman, "Synaptic Characteristics of Ag/AgInSbTe/Ta-Based Memristor for Pattern Recognition Applications," *IEEE Transactions on Electron Devices,* Vol. 64, No. 4, pp. 1806 - 1811, April 2017.

8. Y. Zhang, X. Wang, Y. Li, and E. G. Friedman, "Memristive Model for Synaptic Circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs,* Vol. 64, Issue 7, pp. 767 - 771, July 2017.

9. A. Ciprut and E. G. Friedman, "Modeling Size Limitations of Resistive Crossbar Array With Cell Selectors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 1, pp. 286 - 293, January 2017.

10. B. Vaisband and E. G. Friedman, "Hexagonal TSV Bundle Topology for 3-D ICs" *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 64, No. 1, pp. 11 - 15, January 2017.

11. M. Kazemi, G. E. Rowlands, S. Shi, R. A. Buhrman, and E. G. Friedman, "All-Spin-Orbit Switching of Perpendicular Magnetization," *IEEE Transactions on Electron Devices,* Vol. 63, No. 11, pp. 4499 - 4505, November 2016.

12. B. Vaisband and E. G. Friedman, "Noise Coupling Models in Heterogeneous 3-D ICs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 24, No. 8, pp. 2778 - 2786, August 2016.

13. I. Vaisband and E. G. Friedman, "Stability in Distributed Power Delivery Networks," *IEEE Transactions on Power Electronics,* Vol. 31, No. 28, pp. 5625 - 5633, August 2016.

14. I. Savidis, B. Ciftcioglu, J. Xu, J. Hu, M. Jain, R. Berman, J. Xue, P. Liu, D. Moore, G. Wicks, M. Huang, H. Wu, and E. G. Friedman, "Heterogeneous 3-D Circuits: Integrating Free-Space Optics with CMOS," *Microelectronics Journal*, Volume 50, pp. 66 - 75, April 2016.

15. A. E. Shapiro, F. Atallah, K. Kim, J. Jeong, J. Fischer, and E. G. Friedman, "Adaptive Power Gating of 32-Bit Kogge Stone Adder." *Integration, the VLSI Journal*, Volume 53, pp. 80 - 87, March 2016.

16. Y. Bai, Y. Song, M. N. Bojnordi, A. Shapiro, E. Ipek and E. G. Friedman, "Back To the Future: Current-Mode Processor in the Era of Deeply Scaled CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 24, No. 4, pp. 1266 - 1279, April 2016.

17. M. Kazemi, G. E. Rowlands, E. Ipek, R. A. Buhrman, and E. G. Friedman, "Compact Model for Spin-Orbit Magnetic Tunnel Junctions," *IEEE Transactions on Electron Devices,* Vol. 63, No. 2, pp. 848 - 855, February 2016.

18. J. Wang, N. Gong, and E. G. Friedman, "PNS-FCR: Flexible Charge Recycling Dynamic Circuit Technique for Low Power Microprocessors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 24, No. 2, pp. 613 - 624, February 2016.

19. A. Shapiro and E. G. Friedman, "Power Efficient Level Shifter for 16 nm FinFET Near Threshold Circuits." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 24, No. 2, pp. 774 - 778, February 2016.

20. R. Patel, X. Guo, Q. Guo, E. Ipek, and E. G. Friedman, "Reducing Switching Latency and Energy in STT-MRAM with Field-Assisted Writing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 24, No. 1, pp. 129 - 138, January 2016.

21. K. Xu and E. G. Friedman, "Scaling Trends of Power Noise in 3-D ICs," *Integration, the VLSI Journal*, Volume 51, pp. 139 - 148, 2015.

22. M. Kazemi, E. Ipek, and E. G. Friedman, "Energy Efficient Nonvolatile Flip Flop with Subnanosecond Data Backup Time for Fine Grain Power Gating," *IEEE Transactions on Circuits and Systems II: Express Briefs,* Vol. 62, No. 12, pp. 1154 - 1158, December 2015.

23. I. Savidis, B. Vaisband, and E. G. Friedman, "Experimental Analysis of Thermal Coupling in 3-D Integrated Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 23, No. 10, pp. 2077 - 2089, October 2015.

24. Q. Guo, X. Guo, Y. Bai, R. Patel, E. Ipek, and E. G. Friedman, "Resistive TCAM Systems for Data-Intensive Computing," *IEEE Micro,* pp. 62 - 71, September/October 2015.

25. R. Patel, S. Kvatinsky, E. G. Friedman, and A. Kolodny, "Multistate Register Based on Resistive RAM," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 23, No. 9, pp. 1750 - 1759, September 2015.

26. S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM – A General Model for Voltage Controlled Memristors," *IEEE Transactions on Circuits and Systems II: Express Briefs,* Vol. 62, No. 8, pp. 786 - 790, August 2015.

27. I. Vaisband, B. Price, S. Kose, Y. Kolla, E. G. Friedman, and J. Fischer, "Distributed LDO Regulators in a 28 nm Power Delivery System," *Analog Integrated Circuits and Signal Procesing,* Volume 83, Issue 3, pp. 295 - 309, 2015.

28. I. Vaisband and E. G. Friedman, "Energy Efficient Clustering of On-Chip Power Delivery Systems," *Integration, the VLSI Journal,* Volume 48, pp. 1 - 9, 2015.

29. I. Vaisband, A. Mahmood, E. G. Friedman, and S. Kose, " Digitally Controlled Pulse Width Modulator for On-Chip Power Management," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 22, No. 12, pp. 2527-2534, December 2014.

30. Y. Levy, J. Bruck, Y. Cassuto, E. G. Friedman, A. Kolodny, E. Yaakobi, and S. Kvatinsky, "Logic Operations in Memory Using a Memristive Akers Array," *Microelectronics Journal,* Volume 45, Is-

sue 11, pp. 1429 - 1437, November 2014.

31. M. Kazemi, E. Ipek, and E. G. Friedman, "Adaptive Compact Magnetic Tunnel Junction Model," *IEEE Transactions on Electron Devices,* Vol. 61, No. 11, pp. 3883-3891, November 2014.

32. S. Kvatinsky, D. Belousov, S. Liman, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MAGIC - Memristor-Aided Logic, *IEEE Transactions on Circuits and Systems II: Express Briefs,* Vol. 61, No. 1, pp. 895 - 899, November 2014.

33. S. Kvatinsky, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 22, No. 10, pp. 2054-2066, October 2014.

34. A. Shapiro and E. G. Friedman, "MOS Current Mode Logic Near Threshold Circuits," *Journal on Low Power Electronics and Applications,* Volume 4, pp. 138 - 152, 2014.

35. R. Patel, E. Ipek, and E. G. Friedman, "2T - 1R STT-MRAM Memory Cells for Enhanced Sense Margin and On/Off Current Ratio," *Microelectronics Journal*, Volume 45, Issue 2, pp. 133 - 143, February 2014.

36. S. Kvatinsky, Y. H. Nacson, Y. Etsion, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-Based Multithreading," *IEEE Computer Architecture Letters*, Vol. 13, No. 1, pp. 41 - 44, January-June 2014.

37. I. Vaisband and E. G. Friedman, "Heterogeneous Methodology for Energy Efficient Distribution of On-Chip Power Supplies," *IEEE Transactions on Power Electronics*, Volume 28, Issue 9, pp. 4267 - 4280, September 2013.

38. A. Abdelhadi, R. Ginosar, A. Kolodny, and E. G. Friedman, "Timing-Driven Variation-Aware Synthesis of Hybrid Mesh/Tree Clock Distribution Networks" *Integration, the VLSI Journal*, Volume 46, Issue 4, pp. 382 - 391, September 2013.

39. S. Ge and E. G. Friedman, "Data Bus Swizzling in TSV-Based Three-Dimensional Integrated Circuits," *Microelectronics Journal*, Volume 44, Issue 8, pp. 696 - 705, August 2013.

40. R. Jakushokas and E. G. Friedman, "Power Network Optimization Based on Link Breaking Methodology," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 21, No. 5, pp. 983 - 987, May 2013.

41. S. Kose, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "Active Filter-Based Hybrid On-Chip DC-DC Converter for point-of-Load Voltage Regulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 21, No. 4, pp. 680 - 691, April 2013.

42. I. Savidis, S. Kose, and E. G. Friedman, "Power Noise in TSV-Based 3-D Integrated Circuits," *IEEE Journal of Solid-State Circuits,* Vol. 48, No. 2, pp. 587-597, February 2013.

43. S. Kvatinsky, E. G. Friedman, A. Kolodny, and Uri C. Weiser, "TEAM: ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 60, No. 1,

pp. 211 - 221, January 2013.

44. S. Kose and E. G. Friedman, "Distributed On-Chip Power Delivery," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* Vol. 2, No. 4, pp. 704-713, December 2012.

45. V. Vishnyakov, A. Kolodny, and E. G. Friedman, "Multi-Aggressor Capacitive and Inductive Coupling Noise Modeling and Mitigation," *Microelectronics Journal,* Volume 43, Issue 4, pp. 236 - 243, April 2012.

46. S. Kose and E. G. Friedman, "Efficient Algorithms for Fast IR Drop Analysis Exploiting Locality," *Integration, the VLSI Journal*, Vol. 45, No. 2, pp. 149-161, March 2012.

47. E. Salman and E. G. Friedman, "Utilizing Interdependent Timing Constraints to Enhance Robustness in Synchronous Circuits," *Microelectronics Journal,* Volume 43, Issue 2, pp. 119 - 127, February 2012.

48. B. Ciftcioglu, R. Berman, S. Wang, J. Hu, I. Savidis, M. Jain, D. Moore, M. Huang, E. G. Friedman, G. Wicks, and H. Wu, "3-D Integrated Heterogeneous Intra-Chip Free-Space Optical Interconnect," *Optics Express,* Volume 20, Issue 4, pp. 4331 - 4345, February 13, 2012.

49. V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D Integrated Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 19, No. 12, pp. 2256 - 2268, December 2011.

50. S. Kose and E. G. Friedman, "Effective Resistance of a Two Layer Mesh," *IEEE Transactions on Circuits and Systems II: Express Briefs,* Vol. 58, No. 11, pp. 739 - 743, November 2011.

51. J. Rosenfeld and E. G. Friedman, "Linear and Switch-Mode Conversion in 3-D Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 19, No. 11, pp. 2095 - 2108, November 2011.

52. S. Kose, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 19, No. 8, pp. 1458 - 1468, August 2011.

53. I. Vaisband, E. G. Friedman, R. Ginosar, and A. Kolodny, "Low Power Clock Network Design," *Journal of Low Power Electronics and Applications,* pp. 219-246, 2011.

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May 31, 2019