EVOLUTION OF THE DIGITAL SET TOP BOX

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ABSTRACT

The cost of receivers for digital broadcast services is still high but expected to reduce as new generations of receivers evolve. This paper describes the architecture of the receiver and the devices being used for the implementation of the required functions. It describes some of the issues that new silicon devices are addressing by combining functions in the receiver through integration and providing more efficient solutions. The software architecture is described and how new more flexible techniques are being used to support the downloading of applications and upgrading of receiver software. New features that are expected in the future include more colours in the on-screen display, separate outputs for TV and VCR, higher speed return channels, the use of the DVB Common Interface and the move to digital interconnection of home equipment using IEEE1394.

INTRODUCTION

Digitally broadcast TV services are now well established in markets in many countries. Many of these services have adopted the DVB specifications which have become a world-wide standard. Digital receivers in the form of integrated receiver decoders (IRD), also known as set top boxes (STB), which are needed by the consumer to receive the digital services, have been in manufacture for some time. The cost of digital receivers for DVB services is still predictably high. The costs have not dramatically reduced yet because of three main factors. First, the volumes have not reached really high levels (DSS in the USA is an exception), second because it takes time for the lowest cost implementations to be identified and developed and third because the manufacturing margins so far have been very low or even non-existent. This last reason has come about as a result of the manufacturers having to keep the prices low to enable the market to develop.

New generations of receivers are being developed and manufactured which are bringing both lower costs and increased functionality. This paper takes a look at solutions being deployed in DVB receivers so far and what can be expected in the near future in terms of cost reduction techniques and new functionalities.

DVB INTEGRATED RECEIVER DECODER

The IRD receives and decodes the broadcast TV services. It tunes to the required channel, extracts and decodes the selected data, checks the access rights of the user and outputs picture, sound or other services as needed.

Digital signals are fed to the IRD in the same way as for analogue TV signals so in the case of satellite or MMDS transmission an outdoor unit, comprising dish (or antenna) and low noise block (LNB), is required to receive the signals and convert them to a suitable intermediate frequency (IF). In the case of cable networks or terrestrial VHF/UHF the input to the IRD can be fed directly from the cable network or terrestrial aerial.

Also, similarly, the output video and audio from the digital IRD can be fed to the TV at baseband through a Peritel (21 pin SCART) connection or at UHF with the re-modulated signal fed to the TV tuner.

Most, although not all, of the receivers today include a return channel for communications with a central office. The main use is for the conditional access system however the return channels are also allowing the evolution of narrowband interactive. First IRD’s typically include a PSTN modem with limited speed of 1200 or 2400 baud (V22 or V23bis).

Architecture of the IRD

The main functional blocks of the digital IRD, as shown in the example architecture of Figure 1, can be grouped into the main sub-systems of front-end, conditional access, MPEG decoding (Ref 1), output signal encoding and control with associated I/O.
The CA elements consist of descrambling, some demultiplexing functions to enable decoding of conditional access data in the transport stream, the security module and the means to communicate between the security module and the IRD. These functions may be located together in a self-contained module or they may be contained in devices embedded in the IRD as shown in the example in Figure 2.

Transport packets are selected in the Descrambler using their packet identification number (PID) and descrambled if the scrambling control bits in the packet header indicate they are scrambled. The Microcontroller provides the PID numbers and correct control words supplied by the Smart Card. Entitlement control messages (ECM) and entitlement management messages (EMM) or other CA data carried in the transport stream is extracted by the Demultiplexer and passed to the Smart Card. Decoded control words are returned to the descrambler to enable the descrambling process to be synchronised.

MPEG Decoding and On-Screen Display

The MPEG decoder consists of the system layer decoding (Demultiplexer) and the source decoding (video and audio decoding). Early IRDs implement these in three separate devices plus memory and support circuitry as in the example of Figure 3.

The transport stream contains programmes with elementary streams of video and audio and other data such as PSI, SI, CA information, teletext, etc. The Demultiplexer performs selection and separation of the required streams employing hardware filters where necessary ignoring the streams not required. The video and audio elementary streams are decoded in their respective decoders and data is passed to the
Microcontroller. Video and audio decoding require decompression in hardware due to the complexity and speed necessary to perform the de-compression. More recent IRDs use integrated devices which have combined the video and audio decoding into one device (except for the video memory).

The MPEG video decoder usually has other functions integrated into it for reasons of efficiency. Two of these important functions are aspect ratio conversion and the on-screen display (OSD). Aspect ratio conversion is needed for conversion of 16:9 to 4:3 aspect ratio images, however the necessary interpolation filters are also used to convert from the coded image format to the display format when they differ.

Typically the OSD has the capability to provide 16 colours in any defined rectangular region of the screen using colour look-up tables (CLUT), up to the maximum display resolution of 720 pixels by 576 lines. The regions can not vertically overlap however the CLUT can be changed between regions. Overlay on the video is achieved by putting the OSD information on a plane over the video and making some pixels transparent so that the video appears through the OSD. Pixels which appear transparent are all those outside of any OSD defined regions or those inside an OSD region given a specific colour defined as transparent. This particular approach to OSD has been used as the basis for the DVB specification for sub-titling (Ref 5).

Efficient memory implementation is important to minimise costs particularly for MPEG2 video decoding. Figure 3 shows the MPEG video decoder with 16 Mbits of RAM and the Demultiplexer with an additional 4 Mbits of RAM. This video decoder memory is used for storage of decoded video frames used in the generation of the required output frame and for storing/buffering of other data such as compressed data and OSD data, as shown in Table 1.

<table>
<thead>
<tr>
<th>Data</th>
<th>Memory Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Previous Frame (I or P picture)</td>
<td>4.7 Mbit*</td>
</tr>
<tr>
<td>Current Frame (I, P or B picture)</td>
<td>4.7 Mbit</td>
</tr>
<tr>
<td>Next Frame (I or P picture)</td>
<td>4.7 Mbit</td>
</tr>
<tr>
<td>Compressed Video Buffer</td>
<td>0.6 Mbit**</td>
</tr>
<tr>
<td>On-Screen Display</td>
<td>0.53 Mbit***</td>
</tr>
</tbody>
</table>

* 576 lines x 720 pixels x 4:2:0 sampling x 8 bits.
** 1 frame compressed video due to arbitrary phase of local video sync.
*** 1/3 page (576 lines x 720 pixels) x 4 bits per pixel

Additional memory needs can take the total to more than 16Mbits. Later designs have improved by making more efficient use of this memory. For example first decoders required a complete 3 frames of storage for the previous, next and currently decoded frames as shown. However, improved designs have reduced this to between 2.5 and 2.8 frames which have enabled combined video and audio MPEG decoders to squeeze all their storage into 16 Mbits.

**Output Signal Encoding**

The video encoder performs encoding of the video output of the MPEG decoder (digital Y, Cr, Cb format) to composite (PAL, SECAM or NTSC) and matrixing to R, G, B components. These signals are converted to analogue following which teletext signals are re-inserted in the composite signals if required. The RGB and composite signals are then buffered and fed to the Scart outputs via analogue switches enabling signals coming from a VCR or another decoder to be switched through to the Scart output to the TV.

**Control**

The Microcontroller implements the software (applications, library functions, communications, operating system and the hardware device drivers), sets up the devices in the IRD and controls the I/O ports. It is likely to be a 16 or 32 bit device e.g. Motorola 68K family.

The IRD requires memory for storage of the application code, operating code, working data and configuration data requiring a typical combination of 0.5 Mbyte RAM, 1 Mbyte ROM (FLASH allows upgrading) and 2-8Kbytes Non-Volatile RAM (EEPROM).

The I/O ports of the IRD typically include a serial data interface (RS232) for asynchronous data connection to PC, a parallel data interface (IEEE1284) for higher speed asynchronous data connection to PC/printer, modem return channel for asynchronous data connection to remote device (e.g. a PSTN modem with speeds of 1200 or 2400 baud) and IR receiver for the remote commander.

**Software Architecture and Interactive Services**

Some of the first IRDs are designed with a 'closed' software environment with no easily accessible application interface. The software may be stored in conventional ROM in the IRD so it cannot be upgraded after manufacture resulting in fixed functionality and limited life. The use of reprogrammable ROM such as Flash allows upgrading over the transmission path, through a return channel PSTN modem or other means e.g. via the serial port. However, in order to introduce a new application or to make any change requires replacement of the complete software. This restricts the flexibility and requires duplicated memory to support the upgrade process. To be more flexible the system needs to be able to introduce new applications without
replacing the complete software by dynamic linking of new applications or application modules. This allows new services to be supported by IRDs in the field. Figure 4 shows an architecture to achieve this.

**SCRIPT APPLICATION**

**Script IF**

**INTERPRETER**

**API**

**CORE SOFTWARE**
Including: Real Time Operating System, OSD manager, CA manager, etc.

**DEVICE DRIVERS**

**HARDWARE**

Fig. 4. Download Software Architecture

The application provides the high level control of the IRD e.g. simple channel selection program, electronic program guide or sophisticated interactive software. This is supported by the core software which provides the main software processes such as the OSD manager and CA manager running with a real time operating system. The core controls the hardware through device drivers.

An application programming interface (API) is defined which provides a software interface allowing new application software to be introduced without replacing the layers of software below the interface. In addition, an interpreter provides a means to run script-like applications which don’t have to be compiled into the machine language of the IRD. The application can therefore be standardised across all IRDs from different manufacturers without standardising the core software or real time operating system leaving manufacturers freedom to use their own solutions for these layers of the software. However, the use of Flash memory still provides the capability to upgrade the lower layers if necessary.

The use of the API also means that the scripting language can be upgraded allowing new features or enhancements to be added, again without replacing the complete IRD software. The API as shown needs to support a range of functions in the STB such as presentation of text and objects to the OSD, tuning and selection of programmes, video and audio functions, user command input, conditional access functions, remote communications.

Cost Reduction Through Silicon Integration

![Figure 5 - IRD Cost Breakdown](image)

Figure 5 shows a cost breakdown of the main items in an IRD. Although the digital silicon and memory are the major cost representing about 60% of the IRD, the other parts of the IRD such as power supply, PCBs and housing are also important. Memory costs continue to be driven for the foreseeable future by demand in the computer industry and the available supply. In particular the pricing of DRAM is not easy to predict and has seen very large changes in prices in the last year.

The objectives of integration are to minimise packaging costs, reduce pin count, minimise total silicon areas and achieve architectural efficiencies. In turn the silicon integration leads to other cost reducing benefits in the product such as smaller/less complex PCBs, lower power consumption leading to cheaper power supply design, lower manufacturing costs (less devices to handle, simpler testing) and higher reliability.

Integration of receiver functions started, for example, with the combining of MPEG video and audio decoding, and the integration of the digital part of the front-end into one device. Further silicon integration can be achieved by integrating the DVB descrambler with the Demultiplexer and the Microcontroller (using a RISC core) as shown in Figure 6. An alternative is to create a complete MPEG sub-system but leave the Microcontroller separate. Either approach, with the integration of the video encoder will lead to the final goal of complete integration of the receiver core functions.

![Figure 6 - Integration of Descrambler/ Demultiplexer/ Processor](image)

**RECENT DEVELOPMENTS AND FUTURE TECHNOLOGIES**
Feature Enhancements

New features are being developed which are likely to be introduced into future generations of IRDs. Some of the new features which are expected in the relatively short term i.e. over the next 12 months include:

- **Improved OSD** - 16 colours is the capability that users have come to expect in PCs and it restricts the artistic ability of graphic designers to provide good user interfaces. The move to 256 (8 bit) colours with more flexible transparency (allowing blending of graphics and video) offers much greater potential but will lead to increased memory requirements and increased bit rate requirements.

- **Dual outputs for Scart feeds to TV & VCR** - current IRDs have effectively the same feed to both VCR and TV which means that any OSD used also appears on the recorded version. This is not desirable when viewing the electronic program guide and would be overcome by dual outputs with independent OSD capability.

- **Higher speed modems** - Speeds are likely to increase e.g. to 28.8K baud for PSTN. This will allow the migration to services which are more demanding of bandwidth and require faster response times.

DVB Conditional Access Common Interface

The DVB have defined a conditional access common interface (DVB-CI) (Ref 6) which is in the process of approval by CENELEC. The CASS in the form of a plug-in PCMCIA module contains all the CA elements including descrambling, CA control and the security module (which can still be in the form of a Smart Card plugin in to the module). The complete MPEG transport stream with scrambled packets is passed across the interface to the CASS where selected packets are descrambled and then the complete transport stream is returned to the main IRD. The DVB-CI also has a processor interface for control functions where required e.g. informing the CASS about selected services or asking the IRD to display messages.

Note that although the original purpose of this interface was for CA it can be used for other functions. In particular, capability has been added to the DVB-CI to enable transport streams to be input to the IRD so it could be used for adding a new front-end to an IRD, although issues of module size and power consumption need to be considered.

The Digital Home Bus

The full advantages of consumer digital video equipment will be realised by digital interconnection to the IRD. The high speed digital serial bus specified in IEEE1394 (1994) (Ref 7) was first developed by Apple but has been adopted and endorsed by a large number of industry players and the DVB.

The 1394 bus operates at 100, 200, and 400 Mbps carrying audio, video, data and control signals. This permits several video channels to be carried simultaneously with multiple audio channels and asynchronous data transfers. Standard 1394 signal voltage is 200mVpp to allow battery powered devices to operate, however this limits the distance of any one hop to 4.5 meters. This restricts the use of 1394 to within one room however it is planned to extend the length to reach up to 500m by use of optical fiber(plastic/glass) or UTP (Refs 8 & 9). Note that the cost of a one chip VLSI 1394 interface is expected to be as low as $5 by 1997.

In general, any device can be plugged into any available port on any other device on the bus, up to the limit of 63 devices on one 1394 network, and a maximum of 16 hops between any two devices on the same network. A 1394 home network can be introduced gradually, whereby the user can start with only two devices with 1394 ports and one interconnection between them and build appropriately adding 1394 devices as required.

The 1394 standard cable interconnection comprises 3 pairs of wires, 2 pairs are for half duplex bi-directional signals and 1 pair is for power supply. An alternative version for AV devices has only two pairs without the power. This version is expected to be used for consumer applications.

Figure 7 illustrates the use of 1394 in the home network.

The home has a number of units connected by 1394. It shows a set top box for CATV and satellite, an integrated digital terrestrial TV receiver, PC, Camcorder and DVR. A 1394 bridge is shown to connect between the rooms.
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