EXHIBIT 1004

AREA ARRAY INTERCONNECTION HANDBOOK

EDITED BY

KARL J. PUTTLITZ

PAUL A. TOTTA



Kluwer Academic Publishers
Boston/Dordrecht/London

Distributors for North, Central and South America:
Kluwer Academic Publishers
101 Philip Drive
Assinippi Park
Norwell, Massachusetts 02061 USA
Telephone (781) 871-6600
Fax (781) 871-6528
E-Mail <kluwer@wkap.com>

Distributors for all other countries:
Kluwer Academic Publishers Group
Distribution Centre
Post Office Box 322
3300 AH Dordrecht, THE NETHERLANDS
Telephone 31 78 6392 392
Fax 31 78 6546 474
E-Mail <orderdept@wkap.nl>



Electronic Services <http://www.wkap.nl>

Library of Congress Cataloging-in-Publication Data

The area array interconnection handbook / edited by, Karl L. Puttlitz and Paul Totta
p. cm.
ISBN 0-7923-7919-5
1. Hybrid integrated circuits. 2. Microelectronics. I. Puttlitz, Karl J. II. Totta, Paul.

TK7874.A73.2001
621.3815—dc21

200108653

Copyright © 2001 by Kluwer Academic Publishers.

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means, mechanical, photo-copying, recording, or otherwise, without the prior written permission of the publisher, Kluwer Academic Publishers, 101 Philip Drive, Assinippi Park, Norwell, Massachusetts 02061.

Printed on acid-free paper.

Printed in the United States of America

It is with pl
bored long
and authori
interconnec
We parti
project cou
noted in bo
We also
and MaryA
was in prep

15

Plastic Ball Grid Array

Mark J. Kuzawinski
IBM Microelectronics
Thomas R. Homa
IBM Microelectronics

15.1 Introduction

Plastic Ball Grid Array (PBGA) packages are modules constructed utilizing standard printed circuit card and board technologies. The typical PBGA substrate is a thin (less than 0.035 inches) laminate similar to card technologies used for personal computers. Although the interconnections between a chip and substrate are typically wire bonds, flip-chip dice can be attached to PBGA packages as well. PBGA technologies also support chip scale packaging (CSP) discussed in Chapters 18 and 23.

15.1.1 Evolution of Laminate Technologies for Chip Carriers

Historically, packaging chips on plastic carriers has been limited to the use of metal lead-frame structures, encapsulated in molded plastic, where wire bonds connect the chip to the frame. However, as circuit densities grew during the 1990s, lead-frame technology was severely limited in its ability to support increasing I/O counts since the I/O interconnections were all located at the module perimeter. To increase the I/O count capability of a peripherally-leaded component requires a reduction in lead-frame pitch or increasing the module size. With an ever increasing demand for I/O, it was clear that neither decreasing pitch nor increasing the substrate size provided an acceptable solution, so the area-array concept was adopted.

Early PBGA modules typically consisted of 352 I/O or less. At this stage of the evolution, the industry questioned a switch to PBGAs since lead-frames could adequately handle requirements for 300 or more I/O. However, when demand for I/O counts began to exceed 352, the benefits of an area-array I/O configuration were evident by allowing smaller modules sizes with better electrical performance compared to peripherally-leaded chip carriers. However, fine-pitch, wire-bond technology has significantly extended the I/O range for wire-bond die interconnections. For example, an 8-mm square die can support 168 I/O using a 180-micron pitch, but supports up to 504 I/O at a 60-micron pitch. The trend for fine-wire bond pitches could support even higher I/O counts (1000+). However, the electrical performance of the application could be seriously degraded while an unreasonably large die is required to escape the signals (i.e., provide sufficient perimeter to support high I/O counts).

Table 15-1 PBGA and total package market volumes. (Source: Prismark Partners LLP)

Quantity*	Y1999	Y2004
PBGA volume	1.01	3.63
Total package volume	67.3	105
PBGA market share	1.5%	3.5%

*In billions.

15.1.2 Marketplace Overview

The marketplace has evolved to expect low-cost, high-I/O count plastic packages. The PBGA addresses this need and others. Simple two-layer, chip-up packages are available on a price parity per I/O with lead-frame packages. For a competitive incremental cost, power planes and/or thermal enhancement can also be provided. Wire-bond PBGA packages have dominated the market place due to the lack of an installed flip-chip infrastructure. Many important announcements have been made regarding PBGA flip-chip products, the total volume of these modules steadily increasing as the required infrastructure is established. It is anticipated that wire-bonded dice will continue to dominate low-end PBGA applications and be competitive for some applications requiring high I/O counts as well, made possible by advances in fine and ultra-fine line technology.

Table 15-1 shows the significant percentage of the overall packaging market that is claimed by PBGA products. The PBGA market has grown from emergence in the early 1990s to an estimated 3.7 billion piece market by 2004. Continued growth of the PBGA market is expected past 2004. Chip I/O counts will continue to increase as multiple low I/O count functions are swept into products with higher levels of integration, thereby increasing the off chip I/O requirements.

15.2 PBGA Attributes

15.2.1 Package Standards

JEDEC standard MO-151 [1,2] defines a wide range of PBGA products. It describes chip-up, and cavity-down parts with a variety of I/O pitches and module sizes between 7 and 50 mm per side. Other JEDEC documents [3,4] describe variations of this technology, including chip scale packages (CSPs) and thin modules called low profile ball grid array (LPBGA), that are less than 2-mm high when mounted on a printed circuit card.

15.2.1.1 Marketplace preferences Although the JEDEC standards define a large number of possible product sizes and forms, only a small number of them constructed with specific materials constitute a majority of packages in the marketplace. What is popular in the marketplace of course changes with time. Initially PBGA products typically consisted of 1.5-mm (60 mil) and 1.27-mm (50 mil) I/O pitches [5] migrating to 1-mm grids (and smaller) to avoid the package area from becoming excessive due to rapidly increasing chip I/O counts. In addition to dimensional aspects, material preferences have also emerged. For example, BT (Bismaleimide-Triazine) is the resin of choice for laminate carriers.

15.2.2 Body Sizes and I/O Count

In many cases marketplace preferences have narrowed the large number of possible module sizes to several based on packaging requirements of specific large-volume device types. For example, static random access memory (SRAM) chips typically utilize a 119-I/O, 14 × 22 mm module. Nonmemory applications typically use 27-mm (256 I/O) to 45-mm (672 I/O) body sizes with a 1.27 or 1-mm I/O pitch. One-millimeter pitch modules can provide 672 I/O in a 35-mm body size. There is little demand for plastic array modules smaller than 27 mm, except for chip scale packaging [6]. The I/O counts for several PBGA body sizes configured with four and five rows of solder balls is given in Table 15-2. Chip-up applications, that use thermal balls underneath the die, add from 16 (27-mm body) to 49 (45-mm body) balls to the module I/O counts listed in Table 15-2.

Table 15-2 I/O

Number of Rows	27
4 row	
5 row	

15.2.3 Laminate

Various laminat
in constructing a
tion selection is
tors including c
and wiring comp
can be used for
down modules, w
signal layer and
tion (1S0P), whi
or chip-down m
cross sections a
Fig. 15-1. Just as
logy, additional
nate chip carri



Fig. 15-1 Sc
chip carriers:

Table 15-2 I/O counts for various PBGA body sizes and configurations using 1.27 mm pitch

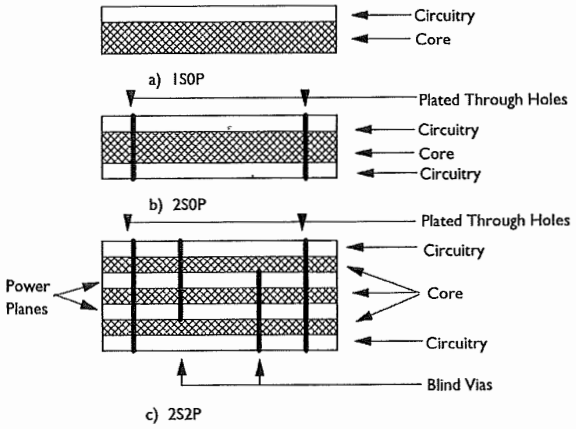
Number of Rows	27 mm	31 mm	35 mm	37.5 mm	40 mm	42.5 mm	45 mm
4 row	256	304	352	400	432	448	496
5 row	—	—	420	480	520	540	600

15.2.3 Laminate Cross Sections

Various laminate cross sections can be used in constructing a chip carrier [7]. Cross section selection is determined by many factors including cost, electrical performance and wiring complexity. Most cross sections can be used for either chip-up or cavity-down modules, with the exception of the one-signal layer and no-power plane configuration (1S0P), which is only suitable for cavity or chip-down modules. The most common cross sections are listed and illustrated in Fig. 15-1. Just as with card and board technology, additional layers can be added to laminate chip carriers. However, use of layer counts over four is just emerging with applications requiring signal redistribution or impedance control. Various card cross sections are discussed in Section 15.3 of this chapter.

15.2.4 Wire Bond and Flip Chip Package Options

The die interconnection practice for PBGA products in the marketplace has been overwhelmingly wire bond due to experience base and infrastructure. For example, PBGA packages have mainly been utilized in low-to-medium I/O requirement applications



1S0P	This cross section places all circuitry on a single layer as there are no inner planes or plated through-holes
2S0P	This cross section provides circuitry on two external layers. There are no inner planes, but plated through-holes are used to connect the two wiring layers.
2S2P	This cross section adds internal layers, typically for power and ground planes. Although defined as two signal and two power planes, all layers can be used for signals or any combination of signals and power.

Fig. 15-1 Schematic representations of various laminate cross sections commonly utilized for PBGA chip carriers: (a) 1S0P, (b) 2S0P, and (c) 2S2P.

which are well suited for wire bonding [8], such as memory packages. However, flip-chip PBGAs are progressing into the marketplace in packages requiring superior electrical performance and to manage high I/O counts.

15.2.4.1 Chip-up, wire bond/flip chip The chip-up PBGA module consists of a substrate on which a die is attached to the 'top' surface and the BGA to the 'bottom' or opposite surface, as depicted in Figs. 15-2a and b. The interconnection can be either wire-bond or flip-chip. Since the die does not constrain the solder ball array surface, chip-up modules can be constructed with a full area of solder ball interconnection to the card or board and can support a higher number of module-to-card interconnections than an equivalent size and pitch cavity down module.

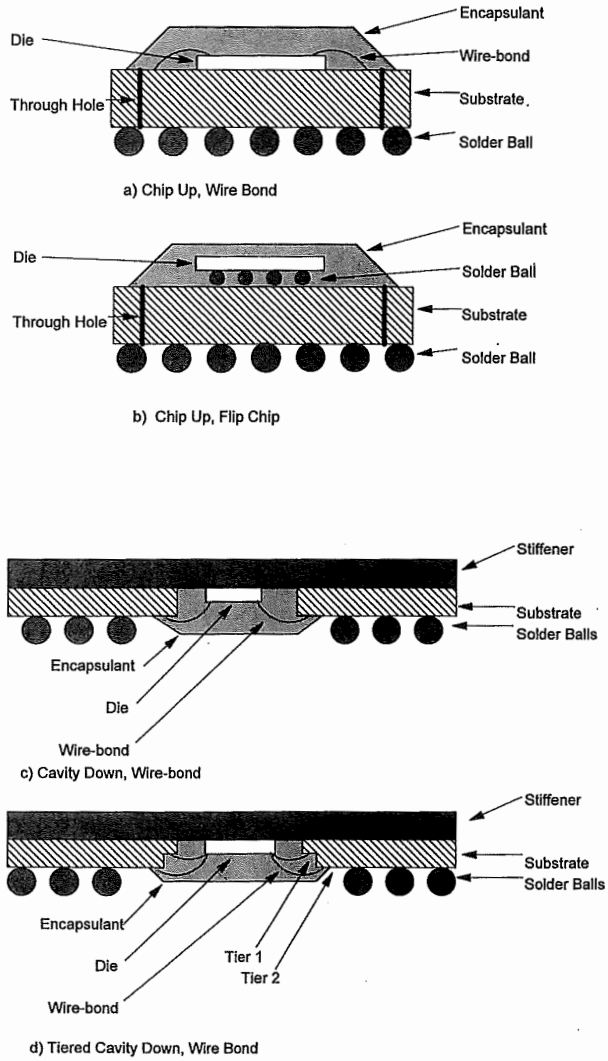


Fig. 15-2 Schematic representations depicting the construction of several common PBGA module types: (a) chip-up, wire bond; (b) chip-up; flip chip; (c) cavity-down; and (d) tiered cavity-down wire bond.

15.2.4.2 Cavity
Cavity-down co
with the die atta
module as the B
Figs. 15-2c and
connection betw
and the card int
same side, heigh
that the encapsu
not interfere wit
array to the card
lem, the die is r
by the laminate
attached to the
is depicted in Fi

Single tier ca
all wire-bonds t
single tier is th
solder ball array
ules have intern
are connected,

Wire bond/fli
designs require
pensed or mo
and the chip fi
Flip-chips are u
joint fatigue l
fill the joints e
from the CTE
(silicon, 3 ppm/
21 ppm/°C).
mechanical and

Thermal diss
sipation is cor
bond package
capsulation us
to use balls u
which is molde
thermal perfor
discussed in Se

15.2.4.3 Var
strates Cavity
used for wire-
area to mount
cation is phys
strate. In othe
nected directl
down module

15.2.4.2 Cavity-down, wire bond/flip chip Cavity-down components are constructed with the die attached to the same side of the module as the BGA solder balls, as shown in Figs. 15-2c and d. Since the chip, the interconnection between the chip and substrate, and the card interconnection are all on the same side, height restrictions must guarantee that the encapsulation over the device does not interfere with the reflow of the solder ball array to the card. In order to avoid this problem, the die is recessed into a cavity formed by the laminate and metal stiffener which is attached to the back side of the module, and is depicted in Fig. 15-2c.

Single tier cavity-down modules connect all wire-bonds to the same plane, or tier. This single tier is the same surface to which the solder ball array is attached. Multi tier modules have internal steps to which wire-bonds are connected, as depicted in Fig. 15-2d.

Wire bond/flip chip features. Wire-bond designs require encapsulation, either dispensed or molded, to protect the wires and the chip from damage after assembly. Flip-chips are underfilled to enhance solder-joint fatigue life because without underfill the joints experience strains that result from the CTE mismatch between the die (silicon, 3 ppm/°C) and the plastic carrier (16–21 ppm/°C). The underfill also provides mechanical and corrosion protection.

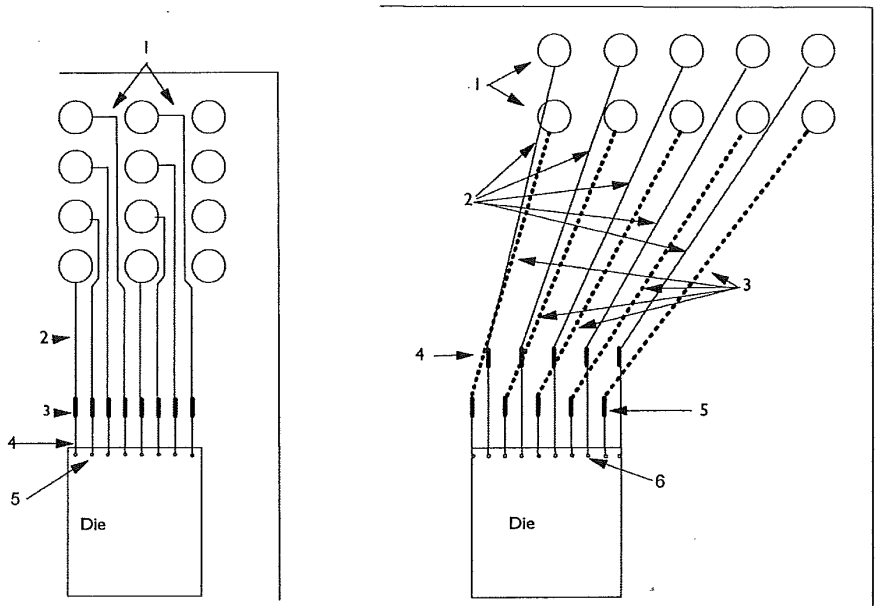
Thermal dissipation. Although heat dissipation is constrained with chip-up wire-bond packages because of the plastic encapsulation used over the die, it is possible to use balls under the die or a heat slug which is molded into the plastic to improve thermal performance. Thermal concepts are discussed in Section 15.7 of this chapter.

15.2.4.3 Variations between cavity substrates Cavity down products can only be used for wire-bond application because the area to mount the chip in a flip-chip application is physically removed from the substrate. In other words, because the die is connected directly to the stiffener in the cavity down module, the flip-chip I/O would be shorted at assembly, rendering the module useless.

Single tier cavity. The single-tier construction is the least complicated cavity-down substrate. It consists of a laminate base with a hole in the center for die placement which is back bonded to the metal stiffener with an adhesive. The laminate can have single or multiple circuitized layers (1S0P, 2S0P, 2S2P, etc.). In order to accommodate the wire-bonds, fine bond finger spacing is required. Although the single-tier, cavity-down substrates are less complicated to construct than multi-tier substrates, they suffer from the disadvantage of less flexible signal wire routing because it is difficult to cross wires to resolve wiring conflicts.

Multi-tier cavity. A multi-tier, cavity-down substrate is constructed using multiple circuit layers laminated in such a fashion as to have a set of "steps" leading out of the cavity on which the bond fingers are placed. The construction of the multi-tier cavity down substrate allows very elegant signal wire routing because each layer of the package can be designed nearly independently of the other, with the only constraint being plated through hole placement which constrains wiring channels. For example, unlike a single-tier substrate where the wiring pattern is typically designed to follow the columns formed by the BGA grid, a tiered-cavity substrate design can be wired either utilizing the columns or the rows defined by the grid. If a suitable number of layers is used, it is also possible to mix the wiring pattern, combining the use of both columns and rows. Figure 15-3 illustrates some of these wiring advantages. An additional advantage of tiered-cavity substrates is that a fine-line technology is not necessary to provide a fine-pitch, wire-bond capability. For example, if a single-tier substrate provides a wire-bond pitch of eight mils, a 2-tier substrate could effectively provide a 4-mil pitch, 3 tiers a 2.66-mil pitch, and so on.

15.2.4.4 No cavity, flip chip down No cavity, chip-down PBGA packages place the



a) single-tier cavity b) multi-tier cavity

Fig. 15-3 Schematic depiction of substrate wiring using columns and rows. (a) Single-tier cavity using wiring in columns, 1-wires in columns, 2-printed circuitry, 3-chip carrier bond fingers, and 4-wire-bonds and 5-die bond pads, (b) Multi-tier cavity using wiring in rows, 1-wiring in rows, 2-surface wiring, 3-internal wiring, 4-top surface bond fingers, 5-bottom tier bond fingers, and 6-die bond pads.

die on the same side of the laminate as the BGA solder balls. Chip-down designs without a cavity are not currently feasible because the total height of the die, wire bonds or solder ball array mounting the chip, and encapsulation of a bonded die would exceed the height of the BGA solder balls.

Cavity-down substrates are typically thermally enhanced through the use of a stiffener which is attached on the top surface of a BGA carrier (Fig. 15-2). The primary purpose of the stiffener is to provide a flat rigid surface to mount the die, and it also serves as a heat sink because it typically is fabricated of metal.

15.3 PBGA Chip Carriers

15.3.1 Single-Layer Carriers

Single-layer substrates utilize a 1S0P cross section with the die mounted on the same side of the substrate as the circuitry [9]. A trade off must be made between power distribution and signal count since both power and signal circuitry compete for the available metal on a single layer. Power connections in single-layer designs are normally placed at the corners of a substrate maximizing the metal available to carry current to the device. However, in consideration of the substrate size, applications with low signal counts may utilize power connections in places other than the corners.

15.3.1.1 Wire bonded and flip-chip packages The term "cavity-down" is utilized for single-layer substrates because the chip, which typically is wire bonded, has a chip cavity on the solder-ball side of a laminate. The cavity provides the necessary height to escape the wire bonds and is filled with an encapsulation material without exceeding the allowable JEDEC-standard defined height. Applications using a flip-chip die can not have a cavity because the chip interconnect requires

that the sub
underneath
in Section
vent this co
application.

Wiring fc
wirebond c
ground ring
Multi-volta
tages by qu
ing (not nec
the substrat
Signal wirin
strained. Tl
wire crossir
Fig. 15-4, w
pear to cros
be resolvec
behind bon
bond finge
ing around
nal wires to
different di

Use of a
(flip-chip) i
wiring confl
by bond-fin

a

Fig. 15-4 S
issue. (a) Th
I/O pad. (Cc

that the substrate wiring be available directly underneath the chip. However, as stated in Section 15.2.4.4, height constraints prevent this configuration from being a practical application.

Wiring for wire-bonded die. Most 1S0P wirebond designs use a single contiguous ground ring with a segmented power ring. Multi-voltage designs either separate voltages by quadrant, or provide power bussing (not necessarily located at the corners of the substrate) to satisfy power requirements. Signal wiring on a 1S0P substrate is also constrained. The wiring is 'point to point' and wire crossing is not allowed. As depicted in Fig. 15-4, wiring conflicts (i.e., wires that appear to cross in a single plane) can sometimes be resolved by designing wiring that loops behind bond fingers, escaping between other bond fingers where necessary, or by looping around BGA pad locations, allowing signal wires to reenter a wiring channel from a different direction.

Use of an area array chip interconnection (flip-chip) may help to resolve some of the wiring conflicts because obstructions created by bond-fingers are no longer present in the design. However, poor placement of signal I/O on a flip-chip die may create the need for wiring underneath the die to resolve the wiring conflicts.

Wiring for flip chip die. The substrate designer can use techniques discussed regarding the wiring for wire-bond die substrates to resolve signal I/O conflicts. However, area array chip interconnection (flip-chip) allows a more elegant wiring solution because wiring may very easily be routed underneath the die to escape where it is required. Just like the wire-bond solution, the ability of the substrate to resolve numerous conflicts is limited because of the single wiring layer being used.

15.3.2 Two-Layer Carriers

Two-layer carriers can be used in either a cavity-down or chip-up configuration. In cavity-down applications, the second layer is typically used as a power plane, although signal wiring can also be placed on that layer. Use of the second layer as a power plane significantly improves the ability of a cavity-down substrate to provide superior power

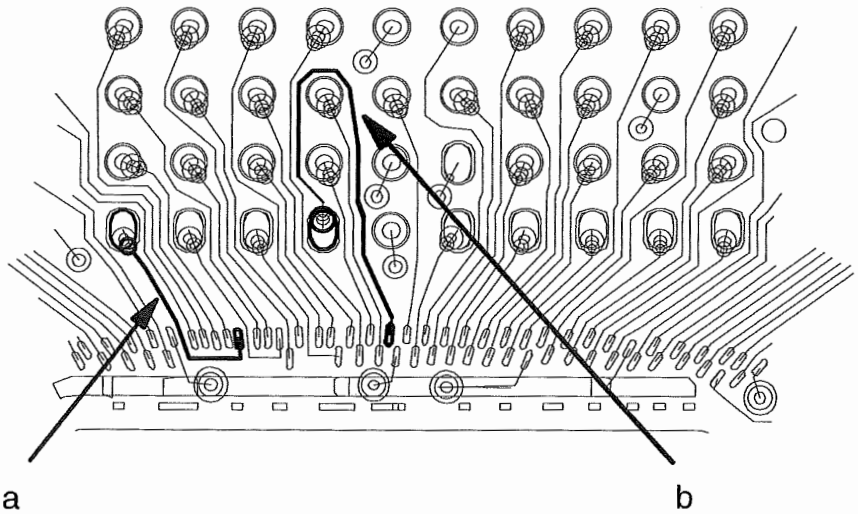


Fig. 15-4 Schematic which illustrates signal trace routing methods used to resolve the wire-crossing issue. (a) The signal trace is looped behind bond fingers. (b) The signal trace is routed around a PBGA I/O pad. (Courtesy of IBM Corporation).

performance compared to a 1S0P design. This is because the entire surface area of the second plane can be allocated to the power distribution, unlike the single layer design where the power distribution typically has less than ten percent of the available area. Chip-up designs also carry power on the second plane, but in a much more constrained fashion because both sides of the substrate are required for signal wiring. Figure 15-5 illustrates some wiring typical of cavity-down and chip-up, two-layer laminates.

15.3.3 *Four-Layer and Greater Carriers*

Four (or greater) layer substrates offer the greatest enhancements for power

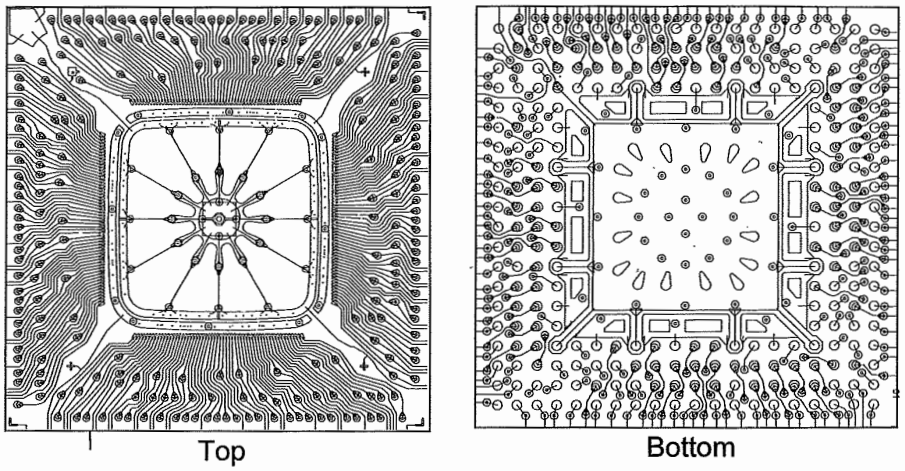


Fig. 15-5 Schematic depiction of two-layer laminate designs. (a) Typical chip-up design, top and bottom layers. (b) Typical cavity-down design, top and bottom layers. (Courtesy of IBM Corporation).

distribution, the greatest flexibility in signal wiring and better heat-distribution characteristics because of the increased metal content in the chip carrier. These substrates allow designers to manage power distribution for multiple voltages, to cross wiring, by moving signals between layers similar to standard circuit card designs, and effectively manage thermal concerns.

15.3.4 Wiring Technologies

15.3.4.1 Subtractive technologies The least complicated and least costly wiring technology available for PBGA applications is a standard subtractive copper-etch process. The process is one where a circuit card is chemically coated with a photosensitive material, exposed to an image and subsequently developed. The development process removes unwanted copper from the circuit card leaving the desired circuit traces. This is the same process used for standard cards and boards and capable of easily circuitizing 3.5 mil line widths and spaces. Some manufacturers subtractive-etch variations can provide features less than 3.5 mils. The current technology limit is 0.7-mil lines and 1.1-mil spaces.

15.3.4.2 Additive technologies Additive technologies, are those that define circuit features by utilizing methods that add metal such as plating on to a laminate carrier rather than etch it away. Additive methods typically provide finer line widths and spaces than subtractive technologies, although some manufacturers have mastered low-cost, fine-line subtractive processes. Additive technologies use the same plated-hole structures that subtractive technologies do, but has the advantage of providing designs with a large number of holes the benefit of using finer lines to simplify routing signal lines.

15.3.4.3 Build up technologies Build-up technologies, such as IBM Corporation's Surface Laminar Circuitry (SLC ™) which is discussed in Chapter 7 of this handbook, provide the designer with the ability to easily escape areas of dense circuit wiring using small diameter blind vias enabling dense flip-chip designs [10,11]. This is made possible by applying layers of thin film dielectric and metal to both sides of a standard laminate core. However, the thin film dielectric material typically has a lower glass transition temperature (Tg) which makes wire-bonding more difficult because the plastic can soften as a wire connection is being made. However, this technology has found many applications in the flip-chip attach arena.

15.3.4.4 Flex technologies Substrates constructed of flexible tape (e.g., Tape Ball Grid Arrays, Chapter 16) are not generally considered to be 'plastic' products.

15.3.4.5 Emerging technologies Other "plastic" technologies presently emerging using Teflon™-based core materials are discussed later in this chapter.

15.3.4.6 Advantages of different wiring technologies The various PBGA chip carrier wiring technologies are summarized and compiled in Table 15-3.

15.4 Wire Bonding Considerations

There are numerous substrate design factors that must be considered in the case

Table 15-3 Comparison of PBGA chip carrier wiring technology attributes. (Dimensions in mils)

		Line Width		Via Diameter		Land Diameter		Bond-finger Pitch	
Method	Cost	min	typ	min	typ	min	typ	min	typ
Subtractive	Low	0.7	3.5	6	12	12	18	5	8
Additive	Medium	1.5	2.5	6	12	12	18	6	6.5
Build-up	High	2	2.5	3	5	5	8	6	7

of wire-bond packages. These considerations include questions about wire-bond length, wire loop height, x-ray or visual inspections, crossing but non-shorting wires, and wire-bond assembly angles to cite a few. All of these considerations require design tradeoffs, where the optimization of one factor causes deoptimization of others.

15.4.1 Geometric Effects

Wire-bonds connecting a silicon device to a substrate exist and function in three dimensions. Most design systems depict wire-bonds in two dimensions, but some performance optimizations can only be made if the design takes into account three-dimensional effects that improve electrical performance (e.g., substrate layout that shortens wire-bond lengths). The drawback to three-dimensional optimization is that visual-inspection processes, such as x-rays, no longer function adequately because the bond wires appear to be shorted in a two-dimensional representation. The following sections illustrate the tradeoffs available to designers for various die pad and bond finger patterns.

15.4.1.1 In-line wire bond patterns A single row of wire-bond bond-pads around the perimeter of the die forms the in-line wire-bond pattern. This pattern, unlike staggered patterns, provides the substrate designer the greatest amount of design flexibility because the single radial pattern of wire-bond wires will not interfere with each other in the 'Z' direction.

Wire lengths. The in-line wire-bond pattern is the most flexible substrate design, but has the disadvantage of having the longest signal wire-bond wires and sharpest angles connecting to pads located at chip corners. The length of a signal wire-bond wire is determined by placing the row of bond fingers on the arc formed between the radials from the chip corners which define the maximum assembly angle, as shown in Fig. 15-6. Depending upon the ground rules established for assembly, the radials defining the arc can

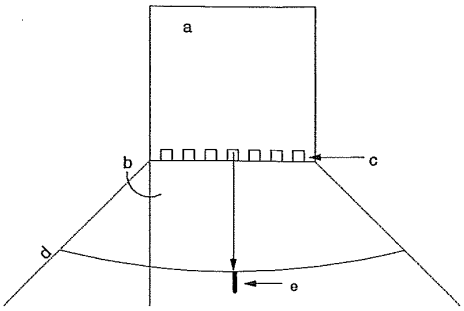


Fig. 15-6 Schematic representation of the maximum wire-bond length and assembly angle for a die with a single row of bond pads and a laminate with a single row of bond fingers: (a) die, (b) 45-degree angle, (c) single row of bond pads, (d) maximum assembly angle radial, and (e) single row of bond-fingers.

be up to 45 degrees off the perpendicular line defined by the chip edge. The actual length of a signal wire is controlled by the total number of signal connections and the pitch of the bond fingers. For example, the length of a wire for a product with 74 signals per quadrant will vary from 72 mils (ignoring power and ground rings) for a 5.1-mil bond finger pitch to 258 mils for a 8-mil bond finger pitch, assuming an assembly constraint of 35 degrees, as depicted in Fig. 15-7.

Loop heights. Loop heights are generally not a concern with in-line patterns because power and signal wires are not in close proximity. X-ray inspection is also not of concern because the design will typically show wires clearly side by side. This happens because each wire-bond wire is next to its neighbor in the X-Y plane and does not cross any other wire. The result of this design concept is a pattern that resembles a hand held fan.

15.4.1.2 Staggered wire bond patterns

Substrate pattern. The width of a substrate bond-finger trace is significantly larger than the width of a circuit line trace. A bond-finger width requirement is put in place to provide a guaranteed minimum flat surface on which to connect a wire-bond. However, the fingers can be staggered to decrease the effective bond-finger pitch of a pattern,

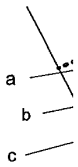


Fig. 15-7 pitch on w sumptions grid, 74 si off-die wi and maxin ous condi 256 mil w (c) 9.6-mr bond-fing pitch, (f) a (h) groun assembly tion of a g absolute r nals. For e first ring : space bet 5-mils, the 70 mils.

thereby with bor requiren where a j is reduc this exa to be a n space be width. U the exa the ove case.

Chip tained if lized on decreasi

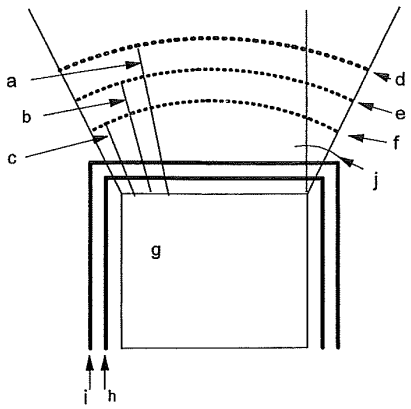


Fig. 15-7 Example of the effects of bond-finger pitch on wire-bond length using the following assumptions: 35-mm body size with 1.27-mm BGA grid, 74 signals per quadrant, 60 micron effective off-die wire-bond pitch, 7.5-mm physical die size, and maximum 35 degree assembly angle. The various conditions represented are: (a) 15-mm arc for 256 mil wire, (b) 12.2-mm arc for 161 mil wire, (c) 9.6-mm arc for 72 mil wire, (d) arc for 8-mil bond-finger pitch, (e) arc for 6.5-mil bond-finger pitch, (f) arc for 5.1-mil bond-finger pitch, (g) chip, (h) ground ring, (i) voltage ring, and (j) maximum assembly angle from orthogonal. The combination of a ground ring and voltage ring defines the absolute minimum wire-bond wire length for signals. For example, if the space from the die to the first ring is 20 mils, each ring is 20 mils, and the space between rings and rings to bond fingers is 5-mils, the resultant minimum signal wire length is 70 mils.

thereby utilizing a narrow wire alternately with bond fingers to calculate the total arc requirement. This is illustrated in Fig. 15-8 where a pattern with a 8-mil bond finger pitch is reduced to an effective 7.3-mil pitch. In this example, the bond fingers are assumed to be a minimum of 5-mils wide, with a 3-mil space between the fingers, and 3-mil line trace width. Utilizing a staggered pad pattern in the example (Fig. 15-8) results in reducing the overall pattern width 8 percent in this case.

Chip pattern. Similar results are obtained if a staggered bond-pad pattern is utilized on a die. Silicon designers are steadily decreasing device feature sizes to increase

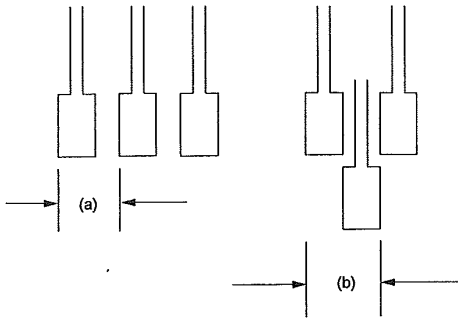


Fig. 15-8 Schematic comparison of in-line and staggered bond fingers. (a) The inline pitch is defined using one bond finger and the space between bond fingers. (b) The staggered bond-finger pitch is defined using one bond finger, the line between bond fingers and spaces that separate the line from the bond fingers and dividing the resultant dimension by two. If the bond finger is 5 mils, then the lines and spaces are 3 mils respectively, the resultant pitch of (a) is 8 mils and (b) is 7 mils.

I/O count and minimize chip size. Package assemblers, however, desire to maintain the passivation opening over the die pad as large as possible to provide the largest diameter wire possible to optimize both the electrical and mechanical properties of the wire. Using a staggered pattern reduces the effective pitch and allows a larger passivation opening similar to the substrate case shown in Fig. 15-8.

Considerations. Although staggered wire-bond patterns aid in easing the pitch density, they significantly complicate the design of a substrate and increase the difficulty of package assembly. Additional loop heights are necessary if a staggered pattern is utilized on either a die, chip carrier, or both, as illustrated in Fig. 15-9. A design advantage but also a visual inspection drawback, is the ability to cross wires using the 'Z' axis. This is possible because of the difference in assembled wire heights as depicted in Fig. 15-10.

15.4.1.3 Wire-bond lengths Substrate designs strive to minimize wire length to enhance electrical and mechanical effects. Wire-bond wire adds greater inductance and

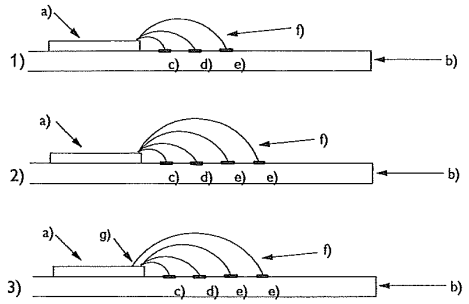


Fig. 15-9 Schematic depiction of wire-bond loop heights for several conditions: 1) in-line die bond pads and bond fingers, 2) in-line die bond pads and staggered bond fingers, and 3) staggered die bond pads and staggered bond fingers. The indicated features are: (a) die, (b) substrate, (c) ground ring, (d) voltage ring, (e) the signal bond-finger(s), (f) the wire bond wires and (g) the second row of staggered die bond pads.

resistance per unit length than substrate circuitry (see Section 15-8). Also, longer wire-bond wires are more flexible therefore subject to droop, and sweep when encapsulated. Excessive wire movement can cause electrical shorting, or breakage resulting in an open circuit. However, using techniques, such as staggered patterns, designers can manage the total length of bond wires.

15.5 Considerations for Flip Chip on Laminate

15.5.1 High and Dense I/O Requirements

Today wire-bond technology continues to offer advantages that make it attractive for the majority of plastic BGA packaging applications. However, flip-chip, area-array interconnections can provide a significant increase in I/O density over wire-bond dice. Figure 15-11 compares wire-bond and full area-array, flip-chip I/O counts for various pitches. The finer the pitch for both types of interconnections, the higher the I/O counts. At the same die size, full area-array dice have a significantly higher I/O count than perimeter wire-bond die and at a much larger pitch. The difference in I/O count between area-array and perimeter-bonded dice increases with increasing die size.

15.5.2 Flip Chip Laminate Carriers

The use of a laminate chip carrier is driven mainly by the ability to accommodate an area-array, flip-chip I/O configuration. In addition, laminate technologies can offer finer line densities, thinner dielectric layers,

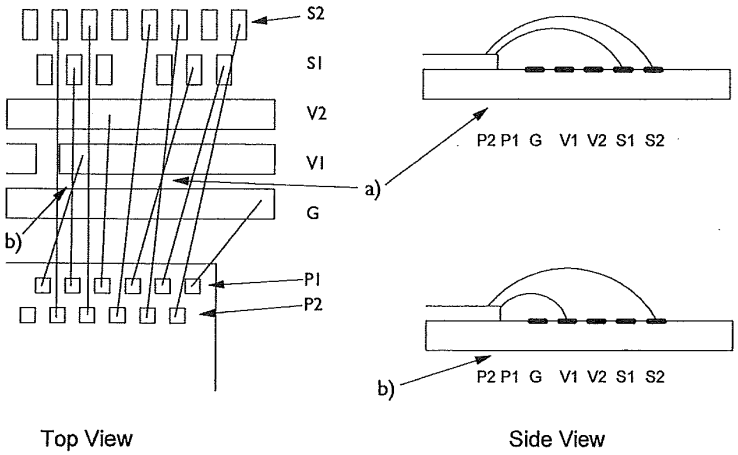


Fig. 15-10 Top and cross-section views of wire-bond examples. (a) Depicts signals crossing as seen in the top view, and (b) is a signal crossing a power connection as shown in the top view. The cross-sectional (side) view clearly shows the seperation in the 'Z' axis illustrating this does not cause an electrical short.

I/O Count

Fig. 15-1 wire bon

and lo to cera nate chi cal perf previou carriers.

There organic benefits liability tion, rol shippin excelle attachm trical p ing, an ume ma process

There carrier PBGA: of simp or built comple

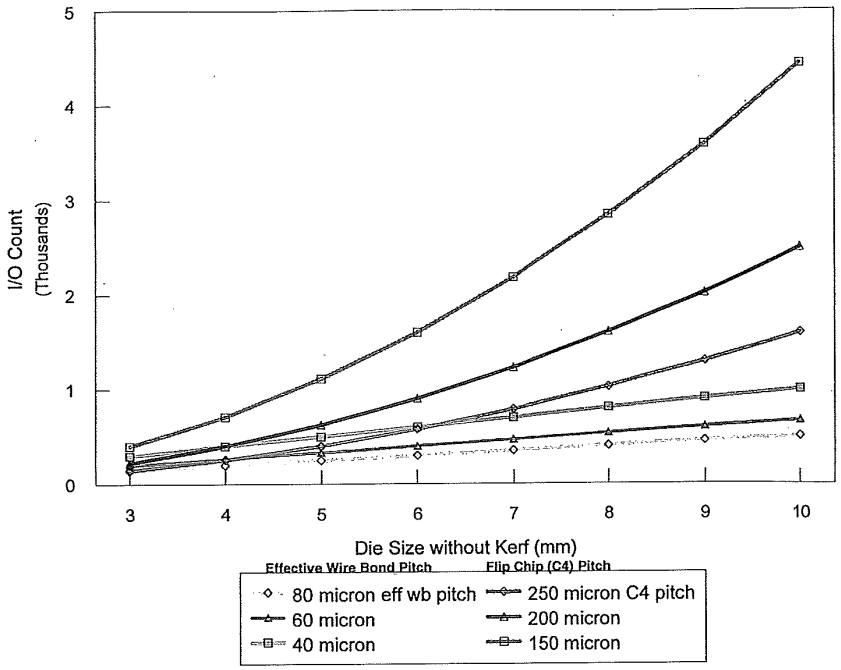


Fig. 15-11 Comparison of the effect of die size on I/O count for full area array flip-chip and fine-pitch wire bond configurations.

and lower dielectric constants compared to ceramic chip carriers. Therefore, laminate chip carriers can meet stringent electrical performance requirements which could previously only be satisfied with ceramic carriers.

There are many advantages to using an organic FC-PBGA package. Some of major benefits of this technology are: improved reliability of the card-to-module interconnection, robust card assembly, robust design for shipping and handling during manufacturing, excellent thermal dissipation via a heat sink attachment to the back of a die, superior electrical performance compared to wire bonding, and being well suited for a high volume mass reflow module and card assembly process [12].

There are three segments found in the chip-carrier marketplace that support flip-chip PBGA modules. These fall into the categories of simple carriers; the medium I/O, fine-line or built-up layer carriers; and high-I/O, high-complexity carriers. These chip carriers have various characteristics which make them suitable for their applications.

15.5.2.1 Chip-down design, no option Unlike cavity-down, wire-bond modules where the die is placed into a recess, the device on a chip-down, flip-chip module is mounted on the bottom surface of a PBGA carrier on the same plane as the solder balls. If, for example, a module with a 1.27 mm grid is used with a ball height after reflow that ranges between 20 to 24 mils, then a thick chip with a 3-mil high interconnection would in most cases make contact with the card to which the module is to be mounted. That is, accounting for warpage during assembly and other manufacturing tolerances, a flip chip will bottom-out on a card. Denser BGA grids of 1 mm or less requiring even smaller diameters (i.e., lower board-to-component height) clearly make a chip-down design impossible to assemble to a card because the chip prevents the solder balls from making contact with the card during reflow.

15.5.2.2 Low I/O flip chip carriers Low I/O chips typically have fewer than 200 interconnections and can be attached to chip carriers whose circuitry is achieved utilizing subtractive techniques (Section 15.3.4.1 Subtractive Technologies). Typically, perimeter I/Os, or perimeter I/Os with a center power core can be supported with these simple substrates. For example, a 10-mm die using a 250-micron interconnection pitch off die and a 1-mm kerf can support 32 I/O per side, or 128 total I/O in a single perimeter row (Fig. 15-12). Up to 120 additional power I/O can be supported inside the outer row, depending upon the number of voltages required and via and land ground rules required for the technology used to design the substrate.

This type of design is geared for low I/O applications since the space between pads dedicated to the chip-to-module interface is not sufficient to support wiring between pads. For example, a 4-mil wire which requires a 4-mil space cannot fit into a 5-mil space between pads which is formed when flip-chip solder joints use a 5-mil pad on 10-mil centers. This is depicted in Fig. 15-12 at arrows g and h.

15.5.2.3 Medium I/O flip-chip carriers The ability to escape both signal and power connections from underneath a flip chip is greatly enhanced by the use of either fine-line

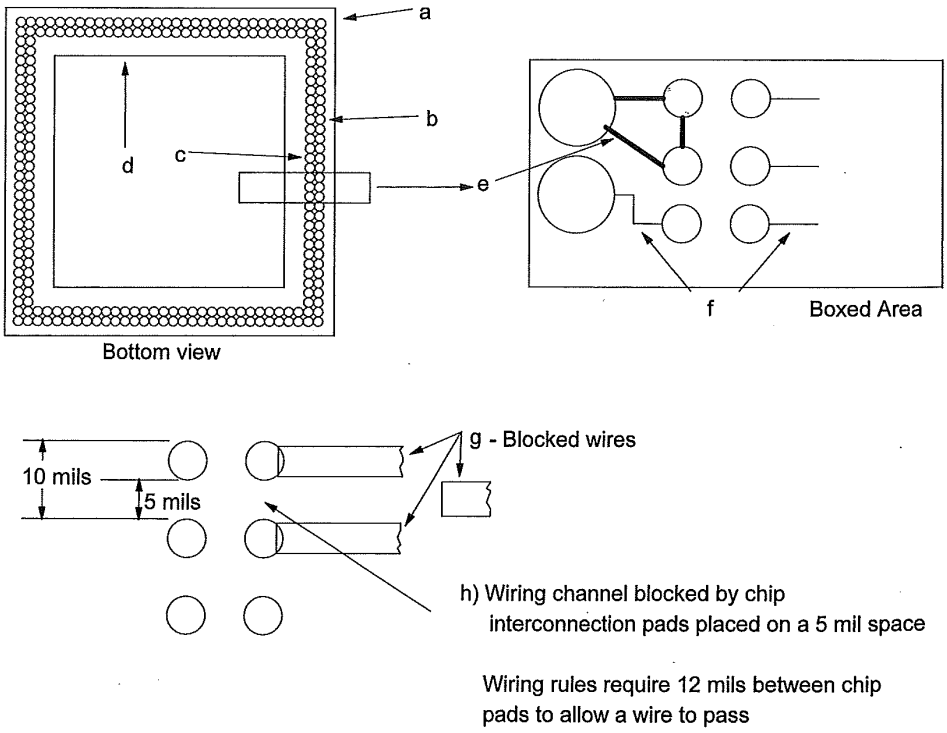


Fig. 15-12 Schematic representation of a highly depopulated low density flip-chip footprint. (a) The chip outline. (b) The outer row of I/O pads. (c) The inner (power) I/O pads. (d) Defines the allowable area for vias used to connect to power bussing. (e) Multiple I/O connect to individual vias beneath the die because the vias are too large for a 1:1 ratio. (f) A limited number of signals can also escape using the path underneath a die, however power performance may be degraded. (g) Depicts 4-mil wiring on 4-mil spaces. (h) Highlights where the wiring contraint occurs.

or build-up technologies (see Chapter 7). In the case of fine-line technologies where 1-mil lines can be circuitized with 1-mil spaces, 2 lines can be escaped between the outer row of C4s if other design constraints, such as maintaining protective coating tolerances are met. Build-up technologies allow the escape of wider lines by stacking these lines one on top of the other. If, for example, a combination of fine lines and build-up technologies is used, five or six perimeter I/O rows can be utilized. For example, in comparison to the case cited in the previous section, again utilizing a depopulated chip (i.e., perimeter versus full area array) allows the number of perimeter I/O to increase from 128 to 624 I/O can be escaped without using drilled vias assuming a six perimeter row implementation, as shown in Figs. 15-13 and 15-14.

Build-up technologies which use micro vias allow wires to be stacked on the surface of a chip carrier and routed between chip pads. This structure is detailed in Chapter 7. Fine wire technologies, which place wires side-by-side on the surface of a chip carrier must support ground rules which assures circuitization of pad and wiring features without interfering with each other.

15.5.2.4 High I/O flip-chip carriers Advanced materials and manufacturing technologies allow plastic substrates to provide full or nearly full area array flip-chip interconnection capability. Not only are fine lines and multi-layer chip carriers used, but small drilled holes, quite often formed using laser drilling techniques, are combined to provide an application with full signal I/O wiring escape. The materials currently used typically are teflon(TM) based.

Escape from underneath a die using small vias is similar to the escape of card to the escape of chip-carrier interconnections to a card. The pattern consists of a short wire from a chip pad to a via, forming a structure with a dog-bone like appearance. Peripheral

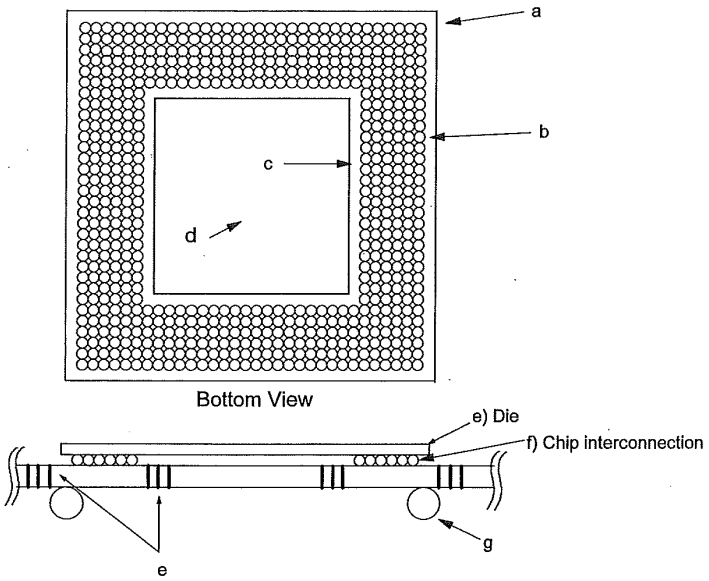


Fig. 15-13 Schematic representation of a depopulated high density flip-chip footprint. (a) The chip outline. (b) The I/O pad matrix. (c) Defines the allowable area for vias used to connect to power bussing which cannot escape with surface wires. (d) Depopulated center portion of the chip. (e) Depicts vias used to escape power and signals from the chip side to the BGA side of the chip carrier. (f) chip interconnections. (g) BGA solder balls. Fine wiring or wiring on build-up layers allow signals to escape between the chip pads, unlike the wiring depicted in Fig. 15-14.

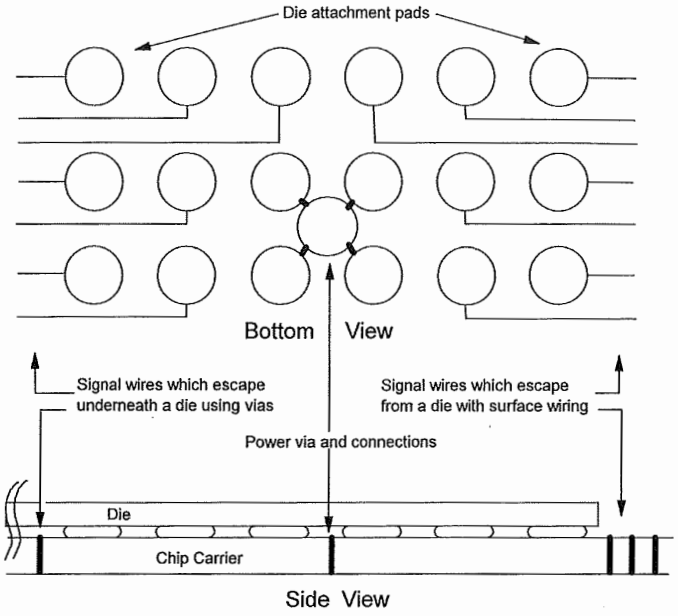


Fig. 15-14 Schematic representation of signal and power escapes underneath the die depicted in Fig. 15-13.

interconnections can be escaped using surface wiring as depicted in Fig. 15-15.

15.5.3 Design Advantages Using Flip-Chip PBGAs

In order to eliminate the shortcomings of wire-bonded plastic BGA-like chip-carriers, such as constrained wiring or reduced electrical performance, the use of flip-chip die-attach can be used as a solution. Chip Carrier wiring improvements are accomplished when obstructions caused by wire-bond rings and fingers are eliminated. Power distribution is improved by eliminating the inductive component of a wire-bond from the die-to-substrate interconnection. A potential side benefit is the reduction in chip-carrier size since the area reserved for wire-bond features can be eliminated.

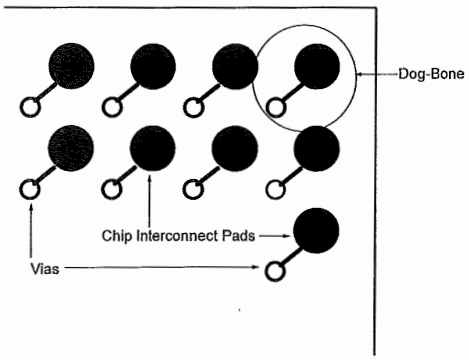


Fig. 15-15 Schematic representation of connections to vias with a dog-bone-like appearance.

15.5.3.1 Fine chip-carrier wiring for flip-chip designs A designer can accomplish design requirements which are not possible or very difficult to accomplish using wire-bond technologies using medium or high I/O flip-chip, chip-carrier designs that utilize fine wires or multi-layer technologies. For example, using a die which has bussing that is divided across two or more quadrants (Fig. 15-16), a design can be implemented which places the bus signals into a contiguous region in one area of the chip-carrier by routing the signal wires underneath the die so that they can be combined with the remainder of the signals forming the bus. This cannot

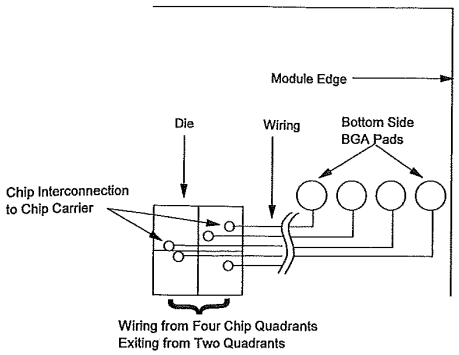


Fig. 15-16 Schematic representation of wiring from multiple chip quadrants escaping to form a single bus on a chip carrier.

be accomplished with cavity-down, wire-bond packages and impractical with chip-up, wire-bond packages because of bond finger and ring obstructions, and a lack of sufficient substrate for wiring in the cavity case.

15.5.3.2 Other advantages Additionally, matched impedance, construction of equal length wiring for differential pairs, and minimized total wiring length are enhanced when using flip-chip designs. For example, as depicted in Fig. 15-17 a flip-chip die mounted on a chip-carrier using solder ball connections can have a wire length measuring approximately the thickness of a laminate cross-section when the via connecting the top and bottom surfaces is directly adjacent to flip-chip and BGA attachment pads. Of course, longer wire lengths result when the BGA pad location is not directly underneath nor adjacent to the die.

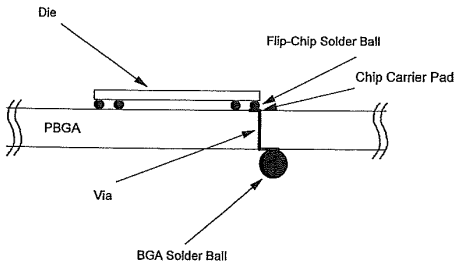


Fig. 15-17 Schematic representation of minimum wire length between a flip-chip solder ball and BGA solder ball.

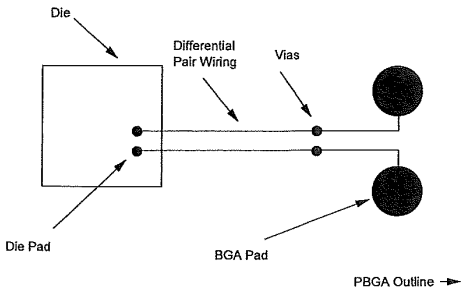


Fig. 15-18 Schematic representation of equal length differential pairs constructed on a chip carrier with a flip-chip die attachment.

15.5.3.3 Differential pairs Differential pairs can be constructed in a similar manner to that shown in the example above, or, if PBGA sites are not located underneath or adjacent to a die, using chip carrier wiring. The wiring length can be precisely controlled because the flip-chip interconnects are assumed to be "next-door-neighbors" as well as the PBGA I/O solder joints to a card. Variations in wire-bond lengths are eliminated, resulting in a pair of wires whose length difference is approximately one-mil (Fig. 15-18).

15.6 Assembly Process Flows

It is important to understand the basic differences in construction of various laminate and module configurations so that the proper technology choices are made for a desired module application. The following sections show some typical process flows, and indicate differences between various options.

15.6.1 Laminate Processing

The chip-up laminate construction (Fig. 15-19) provides the basic structure for either a chip-up or cavity-down chip carrier.

15.6.2 Module Construction

The assembly process flow for wire-bonded modules (Fig. 15-20) is different than flip-chip bonded modules (Fig. 15-21).

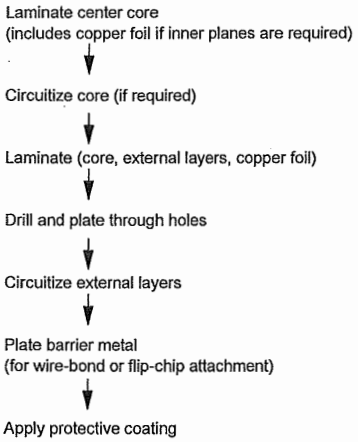


Fig. 15-19 Laminate manufacturing process flow.

15.7 Thermal Performance

15.7.1 Chip Up

15.7.1.1 Wire bonded packages The construction of a chip-up, wire-bond PBGA is inherently resistive thermally because the die is totally surrounded by plastic, which is a thermal insulator. The addition of BGA component-to-board interconnections and a number of thermal vias connected to these BGA connections directly beneath the die improves the thermal performance of chip-up modules by providing a metallic conductive path from the heat source (i.e., chip) to escape to the card. Typically, the majority of the heat from chip-up PBGAs, especially those with thermal balls, is transferred to the card and not the air surrounding the module for dissipation. Some manufacturers have proposed the addition of a heat slug to the chip encapsulation for wire-bond products. This slug is mounted close to but not in contact with the device to prevent damage. Also, the slug must be designed to avoid contact with the wire bonds to prevent electrical shorts.

15.7.1.2 Flip chip bonded packages Flip-chip PBGA packages, typically chip-up, often have a metal lid attached to the back

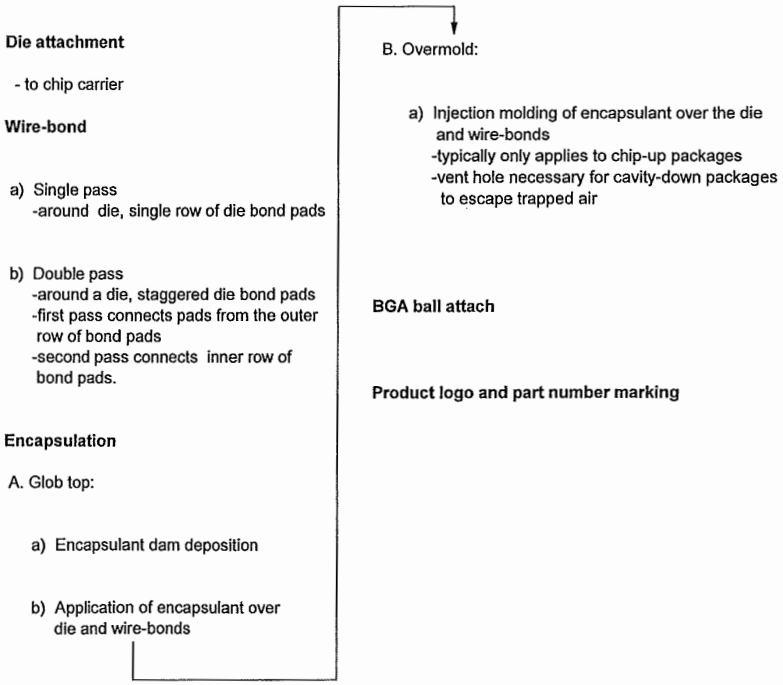


Fig. 15-20 Wire-bond plastic BGA module assembly process flow.

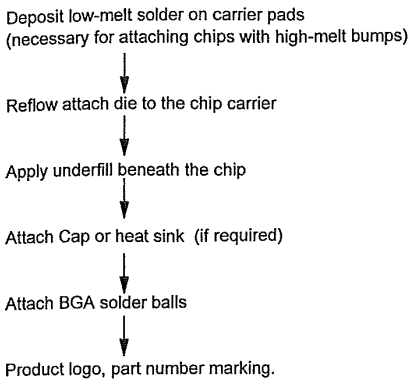


Fig. 15-21 Flip-chip plastic BGA assembly flow.

of the die with an epoxy bond and can provide thermal performance similar to cavity-down wire-bond modules.

15.7.2 Cavity Down

Cavity-down PBGA modules provide an enhanced thermal path to remove heat generated by a die through the use of a metallic lid which also serves as a heat spreader. In a standard cavity-down PBGA construction the die is directly attached to the lid via an epoxy filled with metallic particles to enhance the package's ability to draw heat away from the chip. The combination of transferring heat to a card, and dissipation from the lid to the atmosphere combine to provide cavity-down PBGA modules a significant thermal-performance improvement over chip-up modules. Cavity-down packages are utilized in applications where heat removal is a key consideration. Doing so, however, may require a large body size because of the reduced I/O count made necessary to form the cavity on the module I/O side.

15.7.3 Chip-up versus Cavity-Down Comparison

Although operating voltages are decreasing for each new generation of silicon, power requirements are not following proportionately due to an increased number of off-chip drivers and receivers. Figure 15-22 compares the thermal resistance for various die sizes mounted on a 35-mm chip-up PBGA to

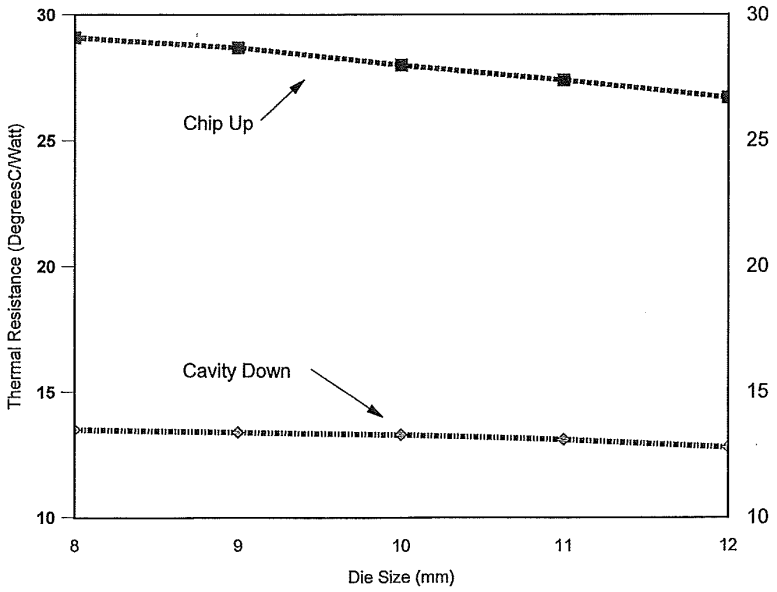


Fig. 15-22 Thermal resistances for various dies sizes between the chip junction and ambient for 35-mm chip-up and cavity-down PBGA chip carriers for the condition of no airflow. (Courtesy of IBM Corp.).

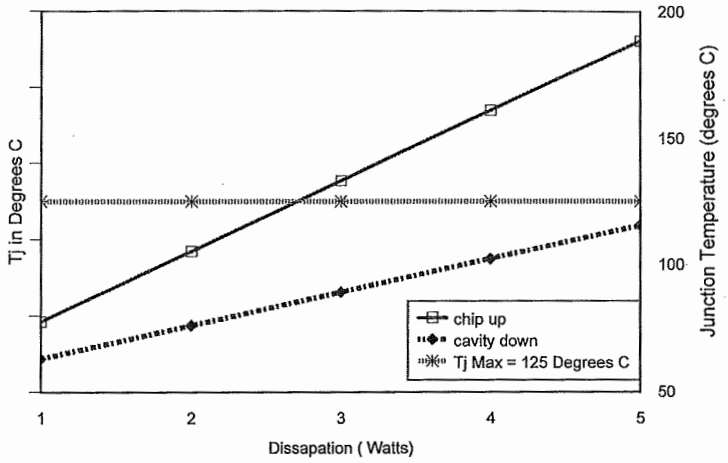


Fig. 15-23 Junction temperatures for chip-up and cavity-down PBGA chip carriers for various power dissipations. Assumes a 50 degree C ambient with no airflow. (Courtesy of IBM Corp.).

similar devices mounted on a 35-mm cavity-down carrier [13]. The module is mounted to a 75-mm square 2S2P circuit card with standard wiring and no thermal enhancements. As indicated, the thermal performance of cavity-down parts is far superior to its chip-up counterpart for all die sizes considered, because cavity-down configurations provide a greater thermal-dissipation capability in PBGA packages [13].

15.7.3.1 Die maximum junction temperature The thermal advantage of a PBGA cavity-down package over a chip-up package is further illustrated in Fig. 15-23, which was generated by taking the average theta j-a for each package in Fig. 15-22 and plotting the junction temperature as a function of chip dissipation. This allows for a comparison of maximum die junction temperature (Tj) between chip-up and cavity-down PBGA packages for any die thermal dissipation. For example, a 125°C junction temperature is quickly exceeded at about 2.5 watts for a chip-up package, while 5 watts can be dissipated by a cavity-down package without forced airflow. At 200 linear feet per minute airflow, a 35-mm cavity-down package, in the application defined above, can dissipate up to 8 watts without a heat sink.

15.7.4 Use of Heat Sinks

The use of heat sinks to help dissipate the power generated by a die is suggested for applications where the maximum allowable device junction temperature will be exceeded. Heat sinks lower the thermal resistance in all cases except where the system is thermally saturated. Thermal saturation is defined in this case to be the situation where heat can no longer be expelled into the environment due to an excessive ambient temperature or excessive system thermal resistance or insulation which prevents proper heat dissipation.

15.7.4.1 Interface integrity vs. reworkability Heat sinks can be attached to modules through the use of an adhesive, clips or other external means. Adhesively attached heat sinks have the advantage of a superior heat-transfer capability because the interface is mechanically consistent and not changed by card warpage, clip fatigue or other mechanical factors. The disadvantage is that in most instances modules cannot be removed for card rework if a heat sink has been adhesively attached. However, systems utilizing heats sinks which are not permanently attached, such as clip attachments, suffer from an interface contact which is less predictable, thus the potential for a lower and less stable rate

Table 15-4 Comparison of signal densities for various wire-bond and flip-chip pitches

Wire bond pitch	115 microns	92 microns	58 microns	40 microns
Percent signals	85	80	75	67
C4 pitch	250 microns	225 microns	200 microns	150 microns
Percent signals	82	80.5	79	77

of heat transfer, but can be easily removed to facilitate card rework.

15.7.5 Modeling

When conducting thermal modeling note that most published thermal-resistance data of PBGA modules is based upon attachment to a 75mm × 75mm square 2S2P circuit card or a JEDEC-defined 104-mm square card. Differences in thermal resistances calculated using the two models are negligible for chips over 10 mm in size and can be ignored in most situations. Applications involving a smaller card area, smaller chip, or different card cross section compared to the standard models need to take these factors into account. The effective thermal resistance of a module increases as the card area decreases from the standard 75-mm square size, and card cross-sectional thermal conductivities change relative to a 2S2P cross-section.

15.8 Electrical Performance

15.8.1 Wire Bond or Flip Chip Die

An important factor in the decision of whether to use wire-bond or a flip chip die often depends upon the electrical performance requirements of the package. Existing silicon technology operates at 2.5 volts with near-term plans of operation at 1.5 volts. In addition to this trend, is the increased percentage of total power connections on a die, especially for wire-bonded applications. As a result of reduced noise margins and lower voltages additional parallel-power connections are required to reduce power-supply source impedance to the chip. As noted earlier die wire-bond connections can pose as a significant electrical constraint for some applications. Flip-chip interconnections provide electrically superior characteristics compared to wire-bonds and necessary for many high-performance applications. Table 15-4 indicates the relative differences in available signal densities for various wire-bond and flip chip interconnection pitches. Flip-chip interconnections solve the electrical and signal densities problems.

15.8.2 Effect of Chip Carrier Wiring

Small die connected to large carriers utilizing fine-line wiring experience larger electrical resistances and inductances compared to smaller carriers due to longer line lengths and narrow traces. The inductance of wires in a high-I/O 55-mm module is compared to a wide-line technology typically used on smaller modules in Table 15-5. The table indicates a wide-line solution can not be built with the same number of signal I/O as a fine-line solution. It is used only to show the electrical effects caused by the mechanical solution [14].

Table 15-5 Net inductance comparison

Electrical Parameters (55 mm module)	2S2P Fine Pitch Wiring	2S2P Standard Ground Rules (Reference)
Zo (Ohms)	79	52
L (nH/in)	13.61	8.85
C (pF/in)	2.64	3.73
Line width/space (mils)	1.5/1.5	4.0/4.0
Wire bond L. (nH) 4 mm	4	4
short wire nH	5.3	3.48
long wire nH	8.6	5.6
Total Net inductance (long wire) nH	12.6	9.6

Table 15-6 Comparison of electrical parameters for several generic PBGA modules with varying pitches and laminate cross sections

Electrical Parameters	1S0P Fine Pitch	2S2P Fine Pitch	2S2P Standard
Zo (Ohms)	142	100	52
L (nH/in)	24.75	16.38	8.85
C (pF/in)	2.34	2.64	3.73
Line width/space (mils)	0.7/1.2	0.7/1.2	4.0/4.0
Wire bond ind. (nH) average	2	2	4

The geometry of the solution which controls the electrical characteristics has one constant and one variable. The constant is the cross-section used to construct the chip carrier as the distance between the signal plane and power plane is pre-defined. The variable is the line width. Decreasing line width causes increased electrical impedance, increased resistance and increased inductance. Although resistance and inductance are a function of the line width, impedance can sometimes be controlled by reducing the distance between the signals and power plane through the selection of a different cross-section.

15.8.3 Tables vs Applications

Of particular interest to circuit designers is the inductance, capacitance and characteristic impedance of a package. However, it is important for circuit designers when comparing technologies not to jump to conclusions regarding the suitability of a package for an application based solely on electrical characteristics cited in tables. The actual packaging application must be analyzed before any decision is made. Consider, for example, the following situation where a designer is provided electrical parameter data comparing the following substrates: a fine-pitch 1S0P cavity-down, a fine-pitch 2S2P chip-up, and a standard (commodity) 2S2P chip-up as listed in Table 15-6. Note that the wirebond inductance is half for the fine-pitch substrates due to the shorter wire length compared to a standard wire-bonded module.

At first glance, the fine-pitch substrates appear to exhibit poor electrical performance based on their inductance and impedance values. However, when comparing electrical characteristics based upon real applications, as listed in Tables 15-7 and 15-8, the values for fine-pitch substrates compare favorably to standard products. Table 15-7 compares 352-I/O substrates while Table 15-8 compares 672-I/O substrates. As would be expected, the 2S2P structures provide similar inductance. If a larger die used on the standard product (9 mm versus 5.9-mm for a 352 I/O package and 16.5 mm versus 10.5 mm for a 672 I/O package) was mounted on the fine-pitch substrates, the total inductance would be reduced even more because of the shorter overall line length.

Table 15-7 Comparison of electrical parameters for several 352-I/O PBGA modules with varying pitches and laminate cross sections

Parameters	1S0P Fine Pitch	2S2P Fine Pitch	2S2P Standard
Package size	27 mm	27 mm	35 mm
Wirebond pitch	60 micron	60 micron	95 micron
Grid pitch	1 mm	1 mm	1.27 mm
Die size	5.9 mm	5.9 mm	9 mm
Average net length (mils)	261	261	333
Net L (nH)	6.5	4.3	2.9
Wire bond L (nH)	2	2	4
Total net L (nH)	8.5	6.3	6.9

EX. 1004 - Page 24

Table 15-8 Comparison of electrical parameters for several 672-I/O PBGA modules with varying pitches and laminate cross sections

Parameters	1S0P Fine Pitch	2S2P Fine Pitch	2S2P Standard
Package size	35 mm	35 mm	45 mm
Wirebond pitch	60 micron	60 micron	95 micron
Grid pitch	1 mm	1 mm	1 .27 mm
Die size	10.5 mm	10.5 mm	16.5 mm
Average net length (mils)	325	325	402
Net L (nH)	8	5.3	3.6
Wire bond L (nH)	2	2	4
Total net L (nH)	10	7.3	7.6

15.8.4 Impedance Matching

With regard to matching impedance on fine-pitch substrates, the overall line length is so short that even a high impedance has negligible effect on reflected noise experienced by a circuit. However, impedance control can be provided by sacrificing some substrate wiring capability as shown in Tables 15-9 and 15-10 which lists the impedance and inductance ground rules for fine-pitch 1S0P and 2S2P cavity-down substrates respectively. Impedance control does not affect the ability to maintain a bond-finger pattern to support 60-micron off-die wiring.

Table 15-9 Comparison of electrical impedance and inductance of a PBGA package with a 1S0P cross section for various fine-pitch geometries

Line width/space (mils)	0.7/1.2	1.5/1.8	3.0/3.5
Zo(Ohms)	142	135	128
L(nH/in)	24.75	21.73	18.83

15.9 Reliability

Reliability in the electronics industry has been defined in many different ways from vague generalities to very precise mathematical definitions.

Table 15-10 Comparison of the electrical impedance and inductance of a PBGA package with a 2S2P cross section for the same fine-pitch geometries evaluated in Table 15-9

Line width/sp (mils)	0.7/1.2	1.5/1.8	3.0/3.5
Zo(Ohms)	100	79	64
L(nH/in)	16.38	13.61	10.88

15.9.1 Reliability versus Quality

Reliability here is defined as the ability of a device or electronic package to perform its intended function over the operating life of the system. Reliability does not require perfection, but operation within predefined failure limits, such as at end of life (EOL) or 95% of the units survive (i.e., not fail) at EOL, or the failure rate specified as some percentage per thousand power on hours. The mathematical treatment of reliability is beyond the scope of this discussion, but are many excellent texts are available on the subject. Frequently "Quality" is used interchangeably with "Reliability." Quality is defined in this chapter as the ability to meet specified dimensions and tolerances, or "fit and finish." It defines how a part appears or performs when it leaves the factory. Reliability on the other hand pertains to how a well a part performs in the field. To illustrate the difference, consider a hypothetical example of a new lap top computer. The case is a snappy pewter, better appearance than the standard black offerings, the screen is bright and easily viewed in direct sunlight, the keys have a crisp snap to your finger pressure, the microprocessor flashes up the required information is fractions of a second. However the hard drive crashes every few months. This is an example of good quality (materials, workmanship) but poor reliability (functionality).

15.9.2 Bonding in PBGA Packages

15.9.2.1 Wire bonded die For plastic ball grid array chip carriers, there are two basic ways to attach a chip to the package. The most widely practiced method is by wirebond, where fine wires individually connect

chip bond pads to corresponding fingers on the chip carrier. The chip is typically attached to the carrier with a conductive epoxy or "die bond" material. There are two basic wire-bond designs, a chip-up version where the device is on the opposite side of the PBGA solder balls, and a chip-down version, where the device is mounted on the same side as the PBGA solder balls. A chip-down device is usually attached to a heat spreader and capable of a higher thermal dissipation than chip-up packages. There appears to be no difference in performance.

Wire-bond chip plastic carriers have been produced in various sizes and material compositions for many years. Even with the anticipated increase in production volumes of flip-chip and direct chip attach (DCA) packages, wire-bond carriers remain the principle interconnection technology. The reasons for this are the existing large wire bonding infrastructure and the fact that wire-bonded packages can be used for many different chip designs. That is the same package can accommodate moderate differences in chip dimensions, and the assembly process steps are very well defined. Also, from a reliability perspective, packages which utilize wire-bonded chips are well understood without unknown failure modes.

15.9.2.2 Flip chip bonded devices For flip-chip carriers, each package must be uniquely defined and cannot be used with different size chips. From a reliability perspective, some questions require resolution before flip-chip plastic packages enjoy the same success as wire-bond modules in standardized stress tests. Specifically, there is a difference in thermal expansion coefficients between a chip and the chip carrier. When a device is turned on, the chip attains a higher temperature than the chip carrier. Even though a chip has a much lower expansion coefficient compared to laminate materials, sufficient strain can be generated between the two materials to cause a fatigue failure mechanism to develop. An underfill material is typically applied between the die and the chip carrier to greatly enhance fatigue resistance. The adhesion to both the die and chip carrier surfaces must be good in order for underfill materials to be effective.

From a card-level reliability perspective, the modulus of an underfill is the most crucial parameter. The overall influence is so great that it changes the effective coefficient of expansion for the area beneath a chip which is visibly distorted. The stress distribution affects the PBGA solder joints under the chip outline and causes these to experience premature failure which is different than ceramic where early failure occurs in joints located near the outside edge of a module.

15.9.3 Standard Stress Tests

15.9.3.1 Acceptable approach The wire-bond PBGA module has been extensively tested and improved until both the individual module and the module assembly provide excellent accelerated stress test results. Because of the international nature of the electronics business, a set of standard tests has been developed to stress packages, and are generally accepted by producers and users alike. It should be understood that passing these tests in not a universal guarantee that plastic chip carriers will meet all reliability requirements over the expected life of a product. However, given the complex nature and effort that would be required to evaluate every application individually, standardized testing is a very acceptable solution. The following tests and test descriptions represent the standardized accelerated stresses applied during a module qualification with the observed criteria for each test [15,16,17, 18,19,20,21].

15.9.3.2 Preconditioning Preconditioning simulates the exposure that a device may experience including environments without humidity control prior to card assembly. When a protective storage bag is opened, plastic components absorb moisture from the air. During assembly, the component temperature is typically 220°C or greater, releasing moisture very rapidly to produce steam, which places a severe stress on the internal structure of a plastic package due

EX. 1004 - Page 26

to the pressure generated. Failures that occur during assembly are known as "pop corning". JEDEC [16] specifications define tests to determine the sensitivity of products to unprotected storage conditions. Level 1 [16] allows a component unlimited exposure whereas Level 6 is the least moisture resistant condition where the component floor life exposure is generally less than 24 hours.

Module test. All modules should be preconditioned to their appropriate JEDEC Level prior to any stressing. Preconditioning consists of drying a component to a base level then placing the part into a humidity chamber defined by the qualification level desired. After exposure for a specified time period, the parts are sent through a reflow oven 3 times to simulate card assembly. Sonoscans are taken of the module before and after preconditioning to determine if any delamination or voids developed during the test. It is expected that changes in module condition do not occur.

15.9.3.3 Accelerated stress tests After preconditioning, plastic BGA-like components can be exposed to a variety of stress tests to determine their ability to withstand specific conditions.

Pressure pot test. This test is designed to demonstrate the ability of a component to withstand very high temperature and humidity. The standard conditions for a Pressure Pot (PP) test is 121°C for 96 or 168 hrs. This is an extremely aggressive test, with particular emphasis on the integrity of resins, adhesives, or components that are sensitive to a very humid environment. Fails normally consist of blistering or delamination in a package, but some active devices are adversely affected by a PP exposure. There has been a trend in the industry to extend the PP test past 168 hrs to demonstrate superiority of a specific product over a competitor. Given the extreme nature of the test, there is no practical advantage to do this since a 96-hr exposure is more than adequate for nearly all applications.

Wet thermal shock. This test is designed to examine the effect of stresses placed on package interfaces caused by the expansion of dissimilar materials. The test consists of two chambers, one with a high-temperature liquid, the other with a very low temperature liquid. The components are cycled between each, allowing time for the parts to reach equilibrium while in each bath. The test has a very high acceleration factor because the liquids allow a very rapid heat-transfer into or out of a component or assembly. The most common stress conditions are −55°C to 125°C although other conditions are given in the JEDEC A-106. A common failure mode is at the interface between a silicon device and encapsulation material. The failure is detected as a Sonoscan void, or less frequently, as an electrical failure. Electrical failures are detected as an open circuit where the failure is a cracked printed wire or broken wirebond. The usual procedure for this test is to electrically test and conduct a Sonoscan on the parts before test, and electrically test after 100, 200, and 300 cycles. Sonoscans are normally performed after the final stress cycle to determine the presence of cracks or delaminations.

Thermal aging. This test is designed to determine how both plastic components and metallic interfaces react to high temperature. This is normally performed at 150°C for 1000 hrs, with intermediate readings at 250 and 500 hrs. The test accelerates changes that normally occur over the lifetime of a system under operational conditions. It is often referred to as the High Temperature Storage Life test (HTSL) and causes degradation of plastic materials, interface failures due to poor adhesive, or release of harmful gasses from plastic materials that attack copper circuitry. The high temperature condition accelerates metallic diffusion processes such as tin from eutectic Sn-Pb solder to react with copper traces. It can also cause aluminum and gold diffusion at chip ball-bonding interfaces to form a destructive intermetallic compound referred to as "the purple plague."

Accelerated thermal cycle test. This test is a moderated version of the wet thermal

shock (WTS) test but is usually performed for 1000 cycles instead of 300. The temperature conditions are usually the same as WTS (−55°C to 125°C) although there are some industry requests for a −65°C to 150°C temperature interval. The ATC test is designed to address interface integrity similar to a WTS test. The testing can be performed utilizing one or two units. The single-unit test, the preferred method, consists of a hot and cold zone with an elevator to move test parts between these zones. Transfer times are very short, so acceleration factors can be large, and the test parts are held at the temperature extremes until they attain a set temperature for a specified dwell period, then the parts are cycled to the other temperature extreme. Parts are electrically tested and a Sonoscan performed at the start of the test, and at 250, 500 and 1000 cycle periods.

15.9.3.4 Temperature and humidity Electronic components are exposed to moderate temperature and humidity conditions with an applied bias to determine the susceptibility for ionic contaminants to migrate between traces and cause electrical short circuits.

Temperature/humidity/bias (THB). The standard test utilized to determine resistance to migration is conducted at 85°C and a relative humidity (RH) of 85% for 1000 hrs with the application of an electrical bias applied at risk sites. A risk site is defined as adjacent conductors with a minimum clearance between them.

Another, more accelerated version of the standard THB test is called HAST for Highly Accelerated Stress Test. The usual conditions for HAST are 130°C at 85%RH for a 96-hour duration. The normal procedure to conduct a THB test is to place the devices into a chamber, allow the humidity to stabilize for 24 to 48 hrs, then turn on the bias. Parts are removed from the chamber at set intervals, normally 250, 500 and 1000 hrs.

In both cases it is prudent to utilize current limiting resistors in a test circuit so potential failure sites are not blown out. Test current should be limited to one micro amp or less.

Assembly test specifications. In addition to module testing, it is good practice to evaluate the module assembled to representative cards to evaluate how the PBGA solder joints perform during standard accelerated thermal cycle (ATC) testing. The test conditions can be identical to the module ATC stress, −55°C to 125°C. The conditions can be reduced to minimize failure within cards which are not related to assembly, such as via and inner-plane connection failures. Electrical readouts are normally conducted at 250, 500, and 1000 cycles. Some manufactures prefer testing at a reduced temperature interval but with additional numbers of temperature cycles, e.g., 0°C to 100°C for 3500 cycles.

Experience has shown that modules may pass module tests, but fail when the assembly is tested as a unit. The principal assembly failure location is usually the PBGA solder joints. It has been determined that normal assembly practices such as reworking adjacent modules on a board, the presence of a heat sink assembly, and double-sided assembly often have a significant impact on module solder-joint life.

Card level assembly. This test is normally performed by initially preconditioning modules through the required JEDEC stress, then passing the packages through two of three reflow exposures. The third reflow stress is used to actually attach the components to a test card. There are several factors to take into consideration from a card assembly point of view.

1. *Card similarity*–The test card assembly should be similar to the application assembly with regard to thickness, construction materials, solder pad design, inner planes, and back side component simulation.

2. *Solder mask*–Solder joint fatigue life of PBGA components is greatly affected by the use of solder-mask capture pads on the card surfaces. The solder mask constricts the solder joint, forming stress-raiser locations when an assembly undergoes temperature cycling stress conditions.

3. *Adhesive*–Also, that the adhesive used to attach heat sinks can greatly reduce

assembly life because the bonded structure is much stiffer than a organic-based module. This composite structure exerts a greater shear force on corner joints causing early fails.

4. *Rework*–Rework of adjacent or backside components can induce bending stresses into the assembly that result in a greatly reduced product life.

15.9.4 Handling Concerns During Test

During a reliability test, module fails can be induced in an otherwise acceptable component by poor handling procedures. Physical damage can be caused in a variety of ways, tainting the test result. With the advent of reduced solder ball pitches migrating from 1.50 mm to 1.27 mm, to 1.00 mm, and below 0.75 mm, solder balls are smaller, bond pads on components are smaller, the circuits are thinner and narrower compared to older, less dense products. Components are becoming increasingly more fragile so care must be exercised when handling them during stress tests.

15.9.4.1 Insertion and extraction of modules from sockets Cracks in printed circuitry, encapsulation or in an organic carrier itself can be caused during the measurement phase of testing if the carrier is flexed during insertion or extraction from a test socket. The flexing motion, which is not typical of an actual circuit application, is caused when a plastic BGA-like component is placed into or removed from a socket attachment mechanism that is not fully in a released position, thus is forced into or out of a socket. The same problem applies when a module is inserted or removed from a test socket at an angle (i.e., not parallel) to the action of the socket.

In addition to cracks introduced into a module by handling, solder balls can be sheared if the module is not inserted or removed from test sockets squarely. The sliding motion of the module over a socket can introduce cracks and may even tear solder balls off a PBGA module. The most vulnerable solder balls to be sheared in this manner are those along the module edge.

15.9.4.2 Use of excessive force for retention in test sockets During qualification testing, it is possible for solder balls to corrode. In order to make good electrical connections for the portions of a test utilized to determine module electrical continuity, some test personnel exert excessive force on a module to drive the socket test probes into the solder balls. Excessive force causes plastic chip carriers to warp and induce cracks in the substrate, circuit wiring and encapsulation. It can also cause the stiffener to delaminate in cavity-down packages.

15.9.4.3 Use of abrasive cleaners for BGA solder balls The proper procedure for electrical test is to clean the solder balls prior to electrical tests to ensure good circuit continuity. However, when the solder balls are cleaned during qualification testing, abrasives such as sand paper should not be used since solder balls can be sheared due to the excessive and uncontrolled force applied. In addition, the use of an abrasive such as sand paper wears down a solder ball, possibly to the point where it no longer makes contact with the socket probe, causing a failure mode not attributable to the module.

15.9.5 Results of Reliability Testing

The results of reliability testing using a standard methodology, such as that defined by JEDEC, provides quantitative data to determine if a design consistently meets a set of defined requirements. However, failure to pass all tests does not necessarily imply that the module is not suitable for an application. Various types of failure observed due to accelerated stress testing laminate ball grid array products are noted in the following sections.

15.9.5.1 Fatigue failure The highest probability failure location for ceramic and plastic BGA-like packages differ. For ceramic BGA-like carriers, solder joints farthest

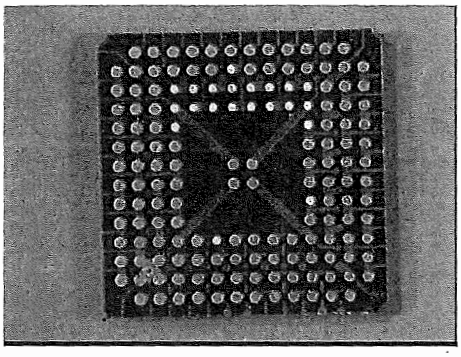


Fig. 15-24 Photograph of the solder joint array side of a flip-chip plastic laminate subjected to accelerated thermal cycle stress testing. Some PBGA solder joints failed (light appearence) located directly below or close to the chip outline on the top side. The chip was underfilled. (Courtesy of IBM Corporation).

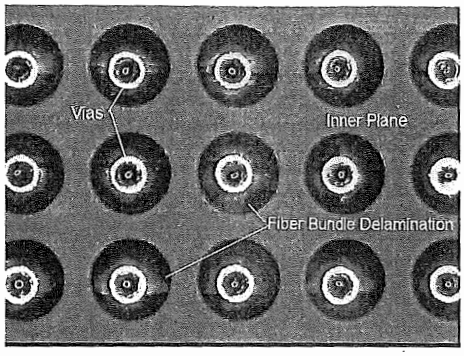


Fig. 15-25 Photograph of a flat (horizontal) cross section of a laminate subjected to a T/H/B (130°C/85%/3.3V) test. Some fiber bundles were observed to delaminate from the base resin. (Courtesy of IBM Corporation).

removed from the center fail first because they obey a distance-from-neutral point (location is dependent of temperature, normally the geometric center) failure relationship. That is, the farther a solder joint is from the neutral point, the greater the strain, and so too the greatest probability for fatigue failure. The strain is caused in part by the mismatch coefficients of thermal expansion (CTE) between a ceramic BGA carrier and the card to which it is mounted. But, this is not the case for plastic BGA-like components since the chip encapsulation and chip itself can significantly influence the local CTE of a laminate, especially if the laminate is thin. Accordingly, for a plastic BGA the package solder joints most prone to fatigue failure are those directly below the die outline, as shown in Fig. 15-24.

15.9.5.2 Laminate degradation Unlike ceramic carriers, laminate carriers are not impervious to the ingress of fluids, including water, which can cause degradation especially under the action of temperature and electrical bias. When problems occur it is not unusual that it involves a discontinuity: resin/fiber interfaces of a laminate, plated through hole (PTH) interface, intersections between circuitry, etc. For example, Fig. 15-25 depicts the horizont l cross-section through a test card used for assembly insulation resistance measurements. Modules were soldered to a typical card, and the assembly placed in a test chamber, 130°C/85%RH with a 3.6 v bias. After 24 to 48 hrs, leakage was discovered on many modules. Failure analysis confirmed that the modules were not failing, but that the leakage was confined to the test card. Flat (horizontal) cross sections through the card showed that fiber bundles delaminating from the base FR4 resin (Fig. 15-25), probably the result of drilling parameters. The bundles connect power planes and through vias. With time and applied bias, leakage paths develop between the vias causing a module to register as a fail.

15.9.5.3 Plated through hole related failures Another laminate-related failure mode observed is plated through hole cracks found in carriers and boards that experience repeated thermal cycles as shown in Fig. 15-26. The figure is an example of a cracked PTH in an assembly test card, a 10-layer FR4 laminate, 0.065″ thick. A 35-mm module was assembled to this card and placed into a −40°C to 125°C accelerated thermal cycle chamber. Fails were detected between 750 and 1000 cycles. Failure analysis indicated that the fails were cracked PTH connections in the test cards caused by Z-axis expansion. Failures of this type can be caused by poor quality copper plating or brittle copper. The PTH copper ductility is a parameter that should be specified for and

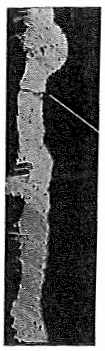


Fig. 15-26
showing c
in a test c
cycle (AT

discussed
where vi
laminate

15.9.5.
those PB
ed die, ar
is the die
wire bon
Fig. 15-2
module s
bonded
to sever
open ci
indicate
were ca



Fig. 15-
bonded c
scan indi
riphery c
Corporat

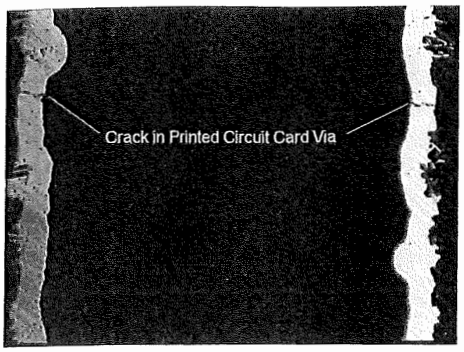


Fig. 15-26 Photograph of a vertical cross section showing cracks in a copper plated through hole in a test card subjected to an accelerated thermal cycle (ATC) test. (Courtesy of IBM Corporation).

discussed with a board vendor in applications where via fatigue due to thermal cycling of a laminate carrier or board could be an issue.

15.9.5.4 Wire bond die attach issues For those PBGA-like packages with a wire bonded die, an issue that continues to be important is the die attachment process, as it for other wire bonded plastic packages. For example, Fig. 15-27 is a sonoscan of a cavity wirebond module showing cracks at the edge of the wire bonded die. The cracks caused several wires to sever resulting in electrical test network open circuits. Subsequent failure analysis indicated that the delamination and cracks were caused by excessive die bond material

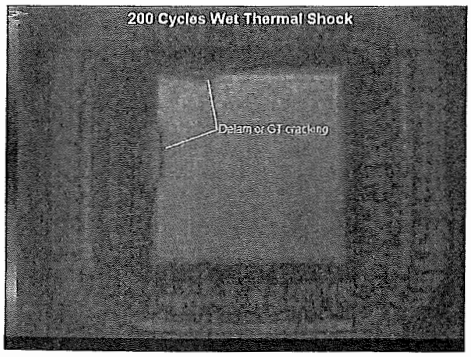


Fig. 15-27 Sonoscan photograph of a wirebonded die mounted in a PBGA chip carrier. The scan indicates delamination and cracking at the periphery of two edges of the die. (Courtesy of IBM Corporation).

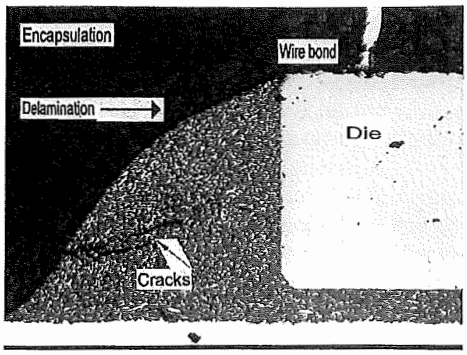


Fig. 15-28 Photomicrograph of a vertical cross section of a wirebonded attachment to a laminate chip carrier. Excess die bond material formed a fillet high on the edge of the die (nearly to the top of the die). Cracks and delamination are indicated. (Courtesy of IBM Corporation).

squeezing out from under the die, forming a fillet on the edge of the die (Fig. 15-28) that very nearly extends to the top of the die. The delamination is barley visible between the die bond material and encapsulation. Some small cracks are seen in the material itself, most likely due to the difference in expansion coefficients between die encapsulant and die bond material. No delamination or cracking has been identified under nominal die bond squeeze out conditions.

15.10 Applications

PBGA substrates offer significant advantages over competing quad flat pack (QFP) technologies. These advantages include impedance control, power planes and advanced thermal management. As with any technology, the advantages can be underutilized, but available for the knowledgeable designer.

15.10.1 "Simple" Chip Up and Cavity Down Designs for Wire-bond Packages

"Simple" designs can be defined as those which can be layed out by a design tool without human intervention. A net list is loaded into a design system which provides a completely wired substrate. Simple wirebond package designs mimic quad flat packs

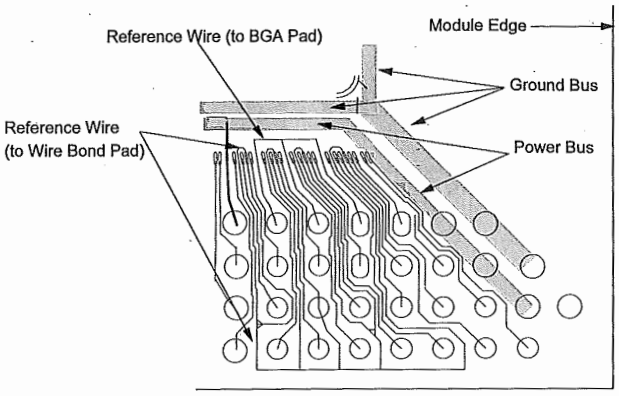


Fig. 15-29 Schematic depiction of a 1S0P layout with electrical shield wires.

and provide a point-to-point wire out. These packages are typically 1S0P cavity or 2S0P chip-up designs that generally have power and ground BGA placement limitations because of the lack of internal power planes. Also, wiring is constrained because it must be routed around the power and ground distribution. 1S0P packages are the most constrained "simple" designs, since power connections are typically required to be placed on the diagonals in the corners of the module. The placement of the power and ground connections in the corners maximizes the surface metallization available for distribution while minimizing the impact on signal wiring as depicted in Fig. 15-29.

15.10.2 "Complex" Chip Up and Cavity Down Designs for Wire-bond Packages

"Complex" PBGA designs run the gamut from wires that cross to signal isolation and multiple wire-bond tiers used to segregate signal busses. Developments in fine-line wiring and small hole drilling technologies have opened the door to nearly unconstrained design capability. Obstructions caused by bond fingers, power and ground rings, BGA sites on cavity-down packages, and size of the land surrounding a via are all design constraints. Complex designs can be the result of a module-size reduction, such as a change from a 672-I/O, 45-mm module on a 1.27-mm BGA pitch, to a 35-mm module on a 1.0-mm BGA pitch. A design shrink, common in microelectronics, can cause severe wiring and feature congestion. In general, complex designs cannot be completed by an automated design system without the aid of designer intervention [22].

15.10.2.1 Crossing signal lines Signal lines that cross can be resolved several ways. A signal trace can be run behind wire-bond fingers and escaped between two fingers at a location which allows access to connect to the desired BGA site (see Fig. 15-4 in Section 15-3). A wire can also be run to the edge of a module and looped around the outermost BGA site or sites and returned to the desired BGA site. Yet another method is to utilize an additional signal layer to cross over to the desired site. In this case, it is possible, although not desirable, to use a power plane to achieve the desired wiring. Examples of the methods described to avoid crossing signal lines are also depicted in Fig. 15-3.

15.10.2.2 Signal isolation Signal isolation can be achieved several ways. Among these is to shield the signal using a strip line, or other similar technique where parallel reference lines surround the signal to be isolated. Another method locates the signal requiring isolation on a separate wiring plane, which can be a power plane. For example, a tiered-cavity part can have a signal plane designated for

EX. 1004 - Page 32

isolated signals where strip lines or isolation could be provided. The simplest approach but least likely to provide a high degree of signal isolation from electrical noise sources is to provide sufficient distances between signal lines. This is an acceptable approach if there is adequate space and requirements are not demanding.

15.10.2.3 Tiers for segregation Tiered-cavity substrates allow the grouping of busses on different layers providing the designer the ability to group signals for optimized card wiring. These groupings can place the signals along a module edge, within a specific row or column, in a block, or within a specified quadrant. Obstructions to wiring on a specific layer are typically not a problem for designers using this type of package.

15.10.3 Card Level Effects on Package Design

Problems associated with bus structures on cards and boards can have an impact upon the design of the substrate. For example, applications with pre-defined I/O to interfaces such as connectors that require the signals on the card to be in a particular order. Problems with this pre-definition occur when the circuitry on the chip cannot be designed to meet the card and board requirements when using standard substrate wiring. In order to meet the requirements of both the chip and the card wiring, the substrate must be able to "cross" wires to resolve any conflicts. Section 15.10.2.1 discusses crossing wiring to meet these needs.

Other considerations are found when using fine pitch BGA grids. For example, a 1.27 mm grid which can support two lines per wiring channel using 5 mil lines and space with a 4.5 mil protective coating tolerance can only support 1 line per wiring channel when using a 1 mm grid. The hidden effect of this comes when analyzing the clearance holes required in the inner planes of the card. If, for example, a five row design is used on a card with 40-mil (1 mm) clearance holes, and only one line per surface channel of wiring is possible, the inner two rows of connections can never be connected to the card power planes because the clearance holes will provide permanent, 10 percent isolation. Signals run to the back side of the card will fill the wiring channel with two lines, effectively isolating the fifth row of connections.

The solution to this problem can be found in either of two design concepts: the first to limit the perimeter rows to four in order to allow wiring to exit under the module or, the second, is to use a technology, such as a build up layer which does not use a drilled via to escape the inner rows of signals.

15.10.4 Fine Pitch Applications

Emerging fine-pitch wiring technologies allow designers to create structures not possible using older, coarser wiring rules. These structures include for example, fine wire-bond finger pitches, increased wires per BGA channel on cavity-down substrates, parallel shielding wires (most beneficial on 1S0P designs), and reduced BGA pitches in high-I/O PBGA substrates [23].

An example, depicted in Fig. 15-29, shows signals isolated from one another with reference lines connected either to power or ground. This design utilizes a fine-pitch wiring technology to provide reference voltages for signals in a 1S0P structure that eliminates the need for a multi-layer cross section for electrical impedance and cross talk control.

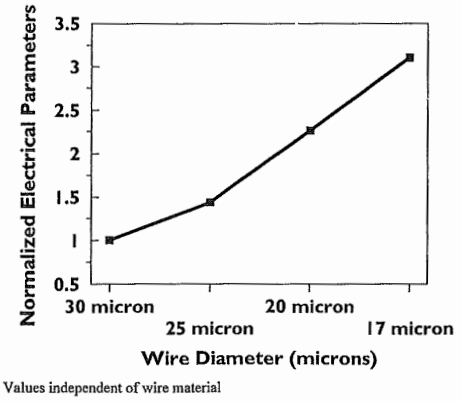
15.10.4.1 Reduced wire diameter implications Off-die pitch reductions of wire-bond products correspondingly necessitate a reduction in the wire diameter used to make connections between the die and substrate. However, thinning the wire adversely affects the electrical characteristics of the connections by increasing resistance and inductance, and also the mechanical properties by softening the wire, making it more susceptible to bowing during encapsulation and causing electrical shorts.

Passivation opening relationship. The opening in the passivation located directly

above the wire-bond pad metalization on a die is directly proportional to the wire diameter used for bonding. A first-order approximation of an appropriate wire-size diameter is one-half of the passivation opening, so a 30-micron diameter would be suitable for a 60-micron diameter opening, a 25-micron diameter wire for a 50-micron diameter opening, and so on. This approximation does not take into account tolerance variances in production, differences in tooling and the like.

Effect on electrical characteristics. The effects of decreasing wire-bond diameter are illustrated in Fig. 15-30 which depicts a normalized plot of electrical parametrics (resistance or inductance) as a function of wire diameter. It indicates as the passivation opening decreases from approximately 60-microns to 35-microns (and wire diameter reduction from 30 to 17 microns per the above relationship) there is a corresponding more than 3-fold increase in electrical resistance and inductance. The increase in resistance due to wire-diameter reduction can be the dominate factor in degrading the electrical characteristics of a package.

Effects on mechanical characteristics. Decreasing wire-bond diameter also degrades mechanical properties. The strength of the wire and its ability to resist bending (sagging) or breakage is reduced as it is thinned.



Values independent of wire material

Fig. 15-30 Effect of decreasing wire bond wire diameter on increasing electrical parasitics (i.e., reducing electrical performance).

The strength of the wire-bond connection to either the die or substrate is also reduced because of the reduced bond area. A reduction in wire diameter can cause other adverse electrical effects such as shorts caused by drooped wires that contact each other, or an open circuit resulting from wire breakage.

15.10.4.2 Tradeoffs between staggered and in-line wire bonding Staggered wire-bond patterns on a die provide an effective way to alleviate many of the mechanical and electrical concerns associated with wire-bond diameter reductions for in-line connections. However, correcting some adverse electrical effects in the package results in problems at the die level. For example, as noted in Table 15-7, electrical performance can be severely impacted by the increase in circuit inductance given the high-frequency switching of modern silicon devices. In order to minimize the electrical degradation caused by wire bonds, high-density products use a double row of die-bond pads to allow for an increase in bond-wire diameter. If the same conditions used to construct Table 15-7 are applied to a double bond-pad design, while using the same 50-micron diameter wire as an electrical reference, it can be shown (ignoring on die effects) that electrical performance can be significantly improved by reducing the circuit inductance (Table 15-8).

Limitations. If the example in Table 15-8 is modified to reflect real silicon by requiring spaces between circuit features and escape from outer bond-pads instead of a Z-axis escape into the device, it would cause additional on-die mechanical trade offs that affect electrical performance. Constraints occur at the inner row of die bond pads, where decisions regarding the space between conductors and the width of conductors affect the pad to which a wire-bond wire is connected. This is illustrated in Fig. 15-31 where two side-by-side bond pads are shown with a circuit trace. Figure 15-32 shows the effect various wire-bond pitches and bond-pad widths have on the circuit trace width, assuming a 5-micron space between the pad and circuitry as indicated in Fig. 15-32. There are

Inner Row Surf
Wiring

Inner Row Die
Bond Pad

Space betweer
Die Pad and Si

Chip Edge

Fig. 15-31
bond pad

diminish
formanc
40 micro
eter and
cases, (w
increase
by decre
respectiv
electrica
Just a
cantly ef
it can als
though a
wires, w
encapsul
open cir

Effect
pattern
rows of
bined tc

Fig. 15-3
pad widt

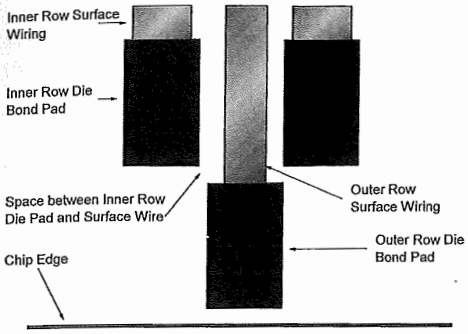


Fig. 15-31 Schematic depiciting straggered wire bond pads on a die.

diminishing returns regarding electrical performance as the wire-bond pitch approaches 40 microns because of the reduced wire diameter and circuit-trace width on a die. In both cases, (wire-bond wire or circuit trace) the increase in resistance and inductance caused by decreasing the metal diameter and width respectively results in a circuit that has poor electrical performance.

Just as wire-diameter reductions significantly effect module electrical performance, it can also severely limit module assembly. Although assembly can be achieved with small wires, wire droop and wire sweep during encapsulation can cause electrical shorting, open circuits due to breakage.

Effective pitch advantage. The staggered pattern of die pads essentially allows two rows of coarse-pitch connections to be combined to provide an effective off-die pitch equivalent to a single row. For example, a 120-micron, single-row pitch translates to a 60-micron effective pitch using two staggered rows. The drawback to a staggered-row concept is that there is a die-pad size reduction penalty. That is, the requirement to provide the widest circuit trace possible from an outer die pad to the chip circuitry dictates that the inner bond pad be reduced in size, as shown in Fig. 15-33. In order to achieve connections to outer pads, the inner pads are required to be smaller, necessitating a reduced wire diameter. There is a benefit to using a staggered pad pattern if the wire diameter shrinks less on a percentage basis compared to the in-line pattern of the same pitch. For example, a sixty-micron inline pad pattern that requires a fifty-micron passivation opening would use a wire of less than 25 microns in diameter while a staggered pattern of 120 microns (sixty effective) would typically use a passivation opening of at least 65 microns allowing a 30 micron diameter wire.

Assembly concerns. Even though the electrical properties and mechanical strength of a wire-bond is improved utilizing a staggered pad pattern due to the wider wire diameter allowed, the pad configuration nevertheless presents some significant assembly concerns, such as crossing wires. Additionally, depending upon the substrate design, wire-bond loop heights can potentially double, causing encapsulation concerns, especially for cavity-down parts. Some substrate designs also stagger bond fingers on the

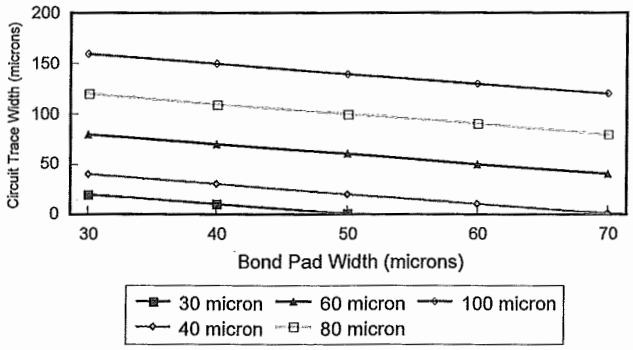


Fig. 15-32 Effect of bond pad width on the circuit trace width between inner bond pads for various pad widths.

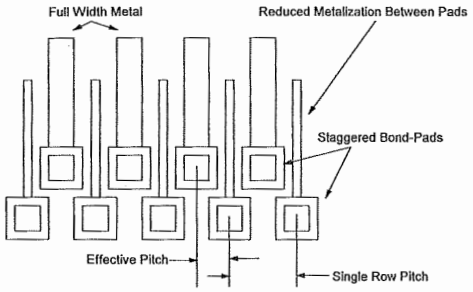


Fig. 15-33 Schematic representation of reduced metallization between staggered wire-bond pads.

laminate carrier, causing yet an additional increase in wire-loop height. Some examples for potential wire crossings are illustrated in Fig. 15-34. This problem arises because the laminate bond-finger pitch is greater than the on-die, bond-pad pitch causing wires to be fanned out in the corners of a die. As shown in the figure, it is possible to lay wires on top of each other creating the risk of electrical shorts if a symmetrical stagger is utilized. However, this situation is avoided with a variable stagger pad pattern, as depicted in Fig. 15-35. By appropriately positioning or stacking die pads in a revised pattern, the wires no longer cross. The use of a stacked pattern becomes increasingly more important as the effective off-die pitch decreases, as noted in Fig. 15-35.

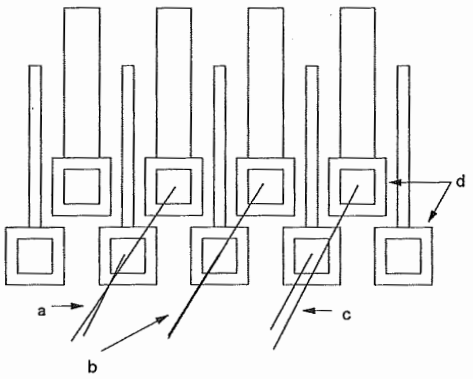


Fig. 15-34 Schematic representation of variable/staggered pitch die bond pads. Features indicated are: (a) crossing wires, (b) overlapping wires, (c) preferred design, and (d) die bond pads.

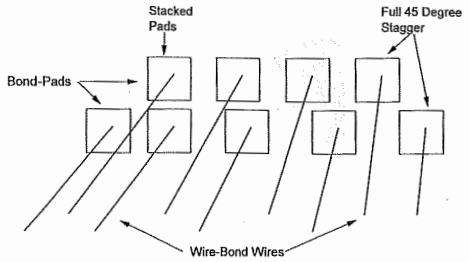


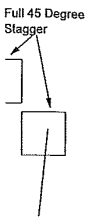
Fig. 15-35 Schematic depicting a variable die bond-pad stagger.

15.10.5 Flip-chip applications

Techniques applied to routing chip-carrier signal wires previously discussed in Sections 15.10.1 and 15.10.2 in the case of wire bonded packages also apply to flip-chip chip-carrier designs. However, there are additional techniques which only apply to flip-chip chip carrier designs discussed in this section.

Presently plastic technologies are evolving to provide Z-axis escape of signals into the internal wiring layers in a manner similar to those found in ceramic substrates. Advanced products, described in Section 15.5.2.4 are providing this capability. However, products with lesser capabilities, such as plastic BGAs aimed at the commodity market with wide lines and spaces, test the imagination of designers due to limitations of these products in their capability of escaping wires from underneath a chip.

15.10.5.1 Low I/O flip-chip applications
Most low I/O flip-chip applications use a single perimeter row of connections between the chip and substrate. The C4 grid typically is on a 10-mil pitch with 5-mil solder-joint pads. Commodity substrates, whose lines and spaces are typically greater than 3.5-mils, do not support wires between pads. If a die is sufficiently large, a second inner row of solder pads can be used and mated to vias located underneath the die. Usually these connections are for power and ground since many flip-chip (C4) pads may be connected to a single common via, relieving congestion beneath a die. It is also possible to wire a limited number of signals directly under a die if there



is sufficient depopulation of the flip-chip array to eliminate congestion underneath the die.

15.10.5.2 Medium I/O flip-chip applications Technologies that provide greater wiring capabilities require the strategic placement of signals and power/ground connections. In order to support the higher wiring densities of these technologies (discussed in Section 15.5.2.3) where the escape is achieved on the chip carrier surface directly beneth the die, provision must be made to allocate sufficient power vias necessary to operate the chip. The schematic representation of Fig. 15-14 depicts this concept. The inner power and ground connections are used in conjunction with power and ground sites located at the perimeter of a device.

15.10.5.3 High I/O flip-chip applications Advanced plastic chip carrier technologies provide nearly limitless combinations of power and signal patterns that are allowed because of the advanced via-formation and fine-line circuitization technologies utilized. Even dense arrays can be escaped without the constraints imposed by surface wiring. This is possible because laser-drilled vias can be as small as 2-mils in diameter. The accuracy of laser drilling also permits significant reductions in feature (land) sizes which allow vias to be placed in C4 pads or in a standard "dog-bone" card design format. These advanced substrates exhibit enhanced electrical characteristics because the materials have lower dielectric constants and an overall reduction in thickness. High-performance transmission lines and differential pairs are easily constructed using these advanced materials.

15.11 Future Extension of PBGA Packages

The future extension of PBGA packages may take on many different forms. High numbers of I/O may force a switch to flip chip if techniques are not found to economically increase the number of wires assembled to a die.

15.11.1 Limitations of Wire Bond Packages

The total I/O count of wire bond packages will be limited, not only by the substrate and its ability to provide bond fingers at a reasonable distance from the die and in a reasonable number, but by the ability of assemblers to connect the additional wires to the die. Also, the limits of acceptable electrical performance are being approached with smaller wire bond wire, as previously discussed, therefore solutions that provide superior electrical performance will be required if additional signal I/O is to be obtained.

Since the total number of I/O on a wire bond package is directly proportional to die size and effective wire bond pitch, and electrical performance is degraded with smaller wire diameters, wire bond packages will be limited in total I/O until such time as silicon allows a 'Z' axis escape from die bond pads. The 'Z' axis escape is required to bypass the congestion of the inner rows of bond pads which narrows the on chip wiring from the pads to unacceptably narrow widths. This advancement will only provide a short extension to the life of high I/O wire-bond applications by mitigating the effects relating to electrical performance. However, just as printed circuits made discrete wiring nearly obsolete in electronic products such as radios and televisions, flip-chip interconnections will do the same to wire-bond products because the costs associated with the proliferation of wires, such as yield loss, will exceed the cost of printed interconnections that are found with flip-chip.

15.11.2 Benefits of Flip Chip Applications

The future of PBGA packages is clearly with Flip Chip applications. Very high I/O counts will be achieved with the use of an area array, which is not practical with a wire bond solution. Further more, unlike the wire bond solution, which will surely degrade in electrical performance with high numbers of I/O, the flip chip solution will provide better power distribution and better signal

performance, both due to the elimination of the discrete wire connection to the substrate.

15.11.3 Challenges to Overcome for Flip Chip PBGA Packages

In order for flip-chip PBGA packages to be available to solve the electrical problems defined above, the packaging industry must invest in new infrastructure to support the volume production that will be required for high-performance organic packaging.

Acknowledgments

The author would like to thank Dr. C. Woychik for his assistance with Section 15.5. The author would also like to thank Mr. S. Engle for his support during the writing of this chapter.

References

1. JEDEC, Electronic Industries Association, 2500 Wilson Blvd., Arlington Va, 22201-3834, www.JEDEC.org.
2. Electronic Industries Association, *JEDEC Outline MS-034 Plastic Ball Grid Array Family Registration*, 2500 Wilson Blvd., Arlington Va, 22201-3834, www.JEDEC.org.
3. Electronic Industries Association, *JEDEC Outline MO-192 Low Profile Ball Grid Array Family*, 2500 Wilson Blvd., Arlington Va, 22201-3834, www.JEDEC.org.
4. Electronic Industries Association, *JEDEC STD 95-1-14 Ball Grid Array Package*, 2500 Wilson Blvd., Arlington Va, 22201-3834, www.JEDEC.org.
5. B. Freyman and R. Pennisi, "Overmolded Plastic Pad Array Carriers (OMPAC): A Low Cost, High Interconnect Density IC Packaging Solution for Consumer and Industrial Electronics," *41st Proceedings Electronic Components and Technology Conference*, pp. 176–182, May 1991.
6. S. E. Lindsey, J. Aday, B. Blood, Y. Guo, R. Hemann, J. Kellar, C. Koehler, J. Liu, V. Sarihan, T. Tessier, L. Thompson and E. Young, "JACS-Pak(TM) Flip-Chip Chip Scale Package Development and Characterizations," *Procceedings 48th Electronic Components and Technology Conference*, pp. 511–517, May 1998.
7. G. Smith, N. Androff, J. Gotro and B. Bedwell, "Advanced Laminate for High Density Interconnect Substrates," *Proceedings Semicon West* (San Jose, CA), Session 6, pp. A1–A9, July 1999.
8. S. Ouimet, J-G. Quintal and G. Robichard, "Wirebonding PBGA Manufacturing Challenges from Fine to Ultrafine Pitch," *Proceedings SEMI Semiconductor Packaging Symposium, SEMICON West* (San Jose, CA) pp. D1–D9, July 1998.
9. M. J. Kuzawinski and K. J. Blackwell, "Ultra Fine Pitch Wire Bond PBGA's," *Electronic Packaging and Production*, vol. 37 (12), pp. 56–62, Sept. 1997.
10. I. Memis, "MicroBGA on Printed Wiring Boards: Recognizing the Need for Surface Laminar Circuit(tm) MicroVia Capability," *Proceedings Semiconductor Packaging Symposium, Semicon West*, pp. F-I–F-8, July 1998.
11. S. R. Tryzbiak and B. J. McDermott, "Photo-Defined Via Technology: Markets, Process and Applications," *Proceedings Semiconductor Packaging Symposium, Semicon West*, pp. G-1–G-9, July 1998.
12. Peter Elenius, "Flip Chip Bumping for Fine Pitch Applications, " *Proceedings The Eleventh Annual Soldering Technology and Interconnection Symposium*, Section 7, Oct. 1998.
13. M. J. Kuzawinski, "Ultra Fine Pitch Wire Bonds: Applications for the Future," *Proceedings Semicon West* (San Jose, CA), Section III, pp. E1–E9, July 1998.
14. Mark J. Kuzawinski, "High Density Wire Bond Packages: Chip Scale and Near Chip Scale PBGAs," Proceedings *International Conference and Exhibition on High Density Packaging and MCMs*, pp. 169–174, Apr. 1999.
15. Electronic Industries Association, *JEDEC JESD Standard 99 Glossary of Microelectronic Terms, Definitions and Symbols*, 2500 Wilson Blvd., Arlington Va, 22201-3834, www.JEDEC.org.
16. Electronic Industries Association, *JEDEC STD A112-A Moisture Induced Stress Sensitivity for Plastic Surface Mount Devices*, 2500 Wilson Blvd., Arlington Va, 22201-3834, www.JEDEC.org.
17. Electi *JESD Cond face* Arlin
18. G. H *of Wi* VA., 1
19. T. R. Pitch *SEMI SEMI* July 1
20. T. R. nate Modu *tor P* pp. D
21. Y. Pa tigue ronm *tor P* (San
22. M. J. plicat 2Q19
23. J. W. "Man strate *ECT*

17. Electronic Industries Association, *JEDEC JESD Standard 51 High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, 2500 Wilson Blvd., Arlington Va, 22201-3834, www.JEDEC.org.
18. G. Harman, *Reliability and Yield Problems of Wire Bonding in Microelectronics*, Reston, VA., ISHM, 1991, p. 28.
19. T. R. Homa, "Reliability Evaluation of Fine Pitch Wire Bond PBGA's," Proceedings *SEMI Semiconductor Packaging Symposium, SEMICON West* (San Jose, CA), pp. A1–A5, July 1998.
20. T. R. Homa, "Reliability Evaluation of Laminate MultilayerUltra Fine Pitch Wire Bond Modules," Proceedings *SEMI Semiconductor Packaging Symposium, SEMICON West*, pp. D1–D12 (San Jose, CA).
21. Y. Pao, X. Song and T. Chung, "Thermal Fatigue of BGA Assemblies in Harsh Environments," *Proceedings SEMI Semiconductor Packaging Symposium, SEMICON West* (San Jose, CA), B1–B18, July 1998.
22. M. J. Kuzawinski, "PBGA Products and Applications," *MicroNews, vol. 4(2)*, pp. 18–19, 2Q1998.
23. J. W. Wilson, R. D. Sebesta and A. D'Alisio, "Manufacturing Ultra Fine Line PBGA Substrates in A PWB Factory," *Proceedings ECTC*, May 1999.

Recommended Reading

1. J. Korleski, R. Gorrell, C. Bowen and D. Nodding, "New Composite Organic Dielectric for High Performance Flip Chip Single Chip Packages," *Proceedings ECTC*, May 1997.
2. T. Chung and I. Yee, "Wafer Level Packaging Technology," *Proceedings SEMICON West* (San Jose, CA), Session 3, pp. A1–A8, July 1999.
3. M. Belazzouz and M. Jimarez, "Process Assembly Development for High Density ASIC Flip Chip/Plastic Ball Grid Array Packages," *Proceedings SEMICON West* (San Jose, CA), Session 5, pp. D1–D34, July 1999.
4. E. Hirt, M. Scheffler and G. Troster, "The Use of Area I/O or a Look on Future Architectures," *Proceedings MCM '99* (Denver, CO), pp. 339–344, Apr. 1999.
5. L. J. Curran, Why Ball Grid Arrays are Picking Up Speed, Semiconductor Business News, *CMP Media Inc.*, http://www.eoenabled.com/edtn/out.asp?n=33586386&i=why+ball+grid+arrays+are+picking+up+speed&url=http%3A%2F%2Fwww%2Esemibiznews%2Ecom%-2Fpub%2F0997%2Fmain%2Ehtm&title=Semiconductor+Business+News+Print+Edition%2C+9%2F97, Sept. 1997.

18

Chip Scale Package Technology

Puligandla Viswanadham
Nokia Mobile Phones, Inc.
Tom Chung
FICTA Technology
Steven O. Dunford
Nokia Mobile Phones, Inc.

18.1 Introduction

In the last three decades, many innovative microelectronics packaging and interconnection-related technologies, such as tape automated bonding (TAB), flip chip, multi-chip modules (MCMs), and ball grid arrays (BGAs), have been developed, applied, and demonstrated in a variety of electronic products. The demand for high-density, high-performance, high-function, portable consumer electronics continues almost undiminished. The ever-increasing demand for product performance, versatility, and miniaturization, resulted in significant advances in semiconductor device power, performance and pin count. These, in turn, have imposed significant challenges upon electronic companies to provide even more compact, cost-effective, and reliable products [1,2].

18.1.1 Background

Chip scale packaging (CSP) is a relatively new packaging technology innovation that was first introduced to industry in approximately 1993. The chip-scale concept was simultaneously proposed by Junichi Kasai of Fujitsu and Gen Mukarami of Hitachi Cable [3] and was demonstrated by Mitsubishi Electric about ten years ago.

18.1.2 Utilization

CSPs can be viewed as an enabling technology for near-term miniaturization for the high-function mobile information processing industry. CSPs are used in a variety of applications where I/O requirements range from 20–289 I/O, encompassing global positioning systems (GPS), flash memory, SDRAM, RDRAM, digital signal processors (DSP), and some logic and ASIC devices. Figure 18-1 indicates that nearly a 90% package area reduction is attainable by migrating from a quad flat pack to a bare die. The technology is believed to be a low-cost alternative to flip-chip attach (FCA) since it may not require underfilling for many applications.

Chip scale packaging has become a very important single-chip packaging technology because an integrated circuit (IC) device can be packaged in a format that is much lighter,

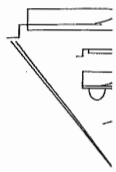


Fig. 18-1 board area ious compo

thinner, a packages ufacturers portable p ers, cellula [4–10].

18.1.3 CSI

CSPs off ate solutio



Fig. 18-2 P footprints.

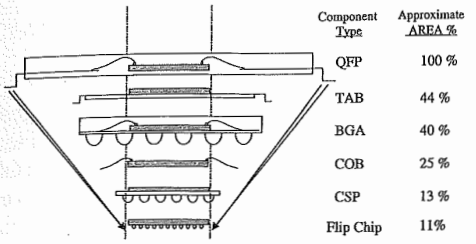


Fig. 18-1 Schematic depicting a comparison of board area requirements necessary to support various components and a bare silicon die.

thinner, and smaller than conventional IC packages (Fig. 18-1). Several, system manufacturers have adopted CSPs for use in portable products such as notebook computers, cellular phones, and digital camcorders [4–10].

18.1.3 CSP vs. DCA/Conventional Packages

CSPs offer an alternative or an intermediate solution to flip chip or direct chip attach technology by enabling the use of current surface mount assembly equipment. In a number of applications an underfill is not required for reliable performance. In fact, the underfill process is a major drawback of direct chip attach (DCA, i.e., flip chip on board) technology. In general, CSPs exhibit improved electrical performance over other packages, and are ideally suited for portable products where size, weight, and robustness are important considerations. A footprint comparison between various BGA and CSP packages, and flip-chip dice is shown in Fig. 18-2, where the bottom sides of the packages are depicted.

The solder balls on area array CSPs collapse to a stand-off height approximately 60 percent of the original ball diameter during solder reflow attachment. Full arrays with selectively removed solder balls and perimeter arrays are typical. Ribbon bonding connects circuitry on a polymer interposer to a die in some designs. While the definition of CSP seems to emphasize the size, the design

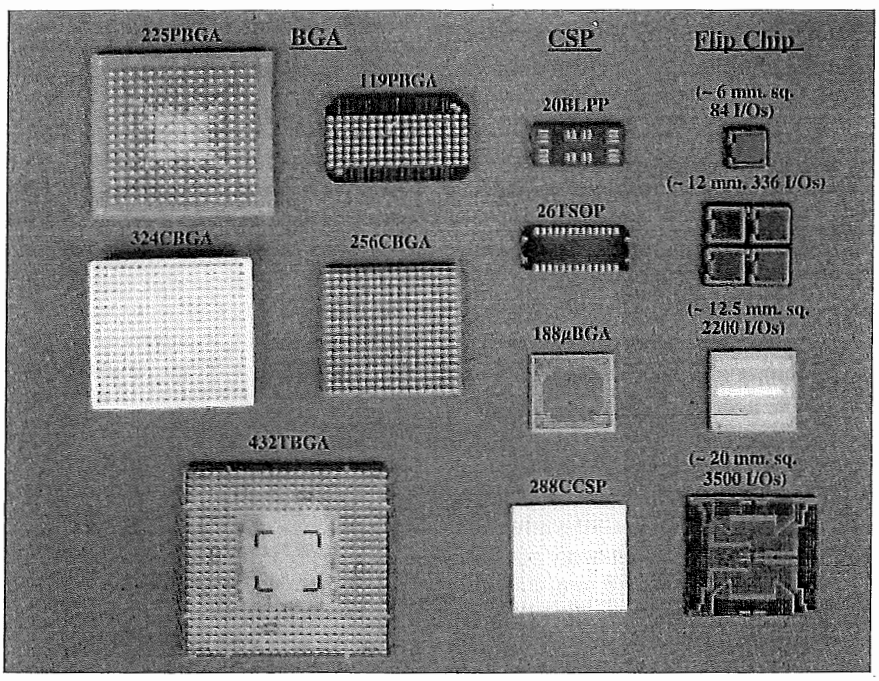


Fig. 18-2 Photograph that depicts the comparative size of chip scale and BGA package outlines and footprints.

and cost of the package depends more on ball pitch.

18.1.4 This Chapter

This chapter is intended to provide an overview of CSP technology including design options and its effects on manufacturability and reliability, key enabling technologies, typical assembly processes, applications, suppliers, and assessment of various CSP technologies [11,12]. Also discussed are the current limitations to CSP application, future trends, and key enablers.

18.2 Chip Scale Package Definition

Chip scale packaging is a single-chip component technology that packages an IC device in a format that is either of the same size or only slightly larger than the IC itself. The Electronic Industries Association (EIA) and the Institute for Interconnecting and Packaging Electronic Circuits (IPC) have jointly set forth a description in the proposed standard, J-Std-012, "Implementation of Flip Chip and Chip Scale Technology." In Section 1.2 of the standard it states:

"Chip scale technology is categorized as semiconductor chip structures that have been made robust to facilitate the ease of chip handling, testing, and chip assembly. The chip scale technologies have common attributes of minimal size, no more than 1.2X the area of the original die size, and are direct surface mountable" [13].

18.2.1 Current Practice

Current practice often stretches the standard definition and this is the case with the CSP definition. Although not technically correct, in practice the term CSP is often very loosely applied to most area-array packages having a pitch of 1.0 mm, 0.8 mm, 0.75 mm, or 0.5 mm, as compared to flip-chip dice whose pitches are 0.5 mm or less. Leaded CSPs are often mistakenly excluded when describing CSPs.

18.3 Package Design Options

Almost 100 different types currently exist in the market with a variety of designs and material sets [14,15]. As an example, Table 18-1 lists key features and references for a number of these CSP designs. They have common attributes of minimal size; no more than approximately 1.5X the area of the original die size, and are directly surface mountable. These packages are designed to be assembled using conventional assembly tools and solder-reflow processing. Thus, CSP technologies target the form factor, high density, and high performance of direct chip attachment, but with a mechanically protected body useful for handling and burn in, and not requiring underfill in many cases.

18.3.1 Distinction From DCA

The main distinction from direct chip attach (DCA/FCA) is that there is still some packaging involved. This is accomplished by the addition of material layers, or interposers between the silicon and substrate or board, which serve as compliant members, space transformers, and mechanical protection for the dice. CSPs are categorized into four types depending on the nature of the interposer and construction: lead frame, flexible interposer, rigid interposer, and wafer-level processed CSPs as illustrated in Fig. 18-3. A brief description of each type is provided in the following sections along with typical examples. Information about CSP manufacturers, interposer material, die-to-interposer connection, and external-connection structure for each CSP type is listed in Tables 18-2 through 18-5 [61].

18.3.2 Lead Frame

This type CSP utilizes custom-designed lead frames, where the original purpose was to provide a method of stacking chips to enhance memory capacity. Since then a variety of forms have come into existence, among them are: Lead-On-Chip (LOC),

Table 18-1

Sup
[Published

Chip Scale
[16,17,47
EPS
[46,50,51
Fujitsu [18
GE [21,54]
IBM [22]
LG Semic
[23–25,1
Matsushit
[26,27,2
Mitsubishi
[29,30,3
Motorola
[32–34,4
NEC [35]

Nitto Den
Sandia/A
[37,131]
ShellCase
Tessera/A
Shinko
[40–42,
TI Japan
[4,43,49
Toshiba [

Small O
Outline
Package
etc. [62].
in Fig. 1
moved ir
the lead
device, a
thick, dc
intercon
frame is
The asyr
with epo
formed
tom lea
of lead-
several

Table 18-1 Various chip scale package technologies described in the literature

Supplier [Published Reference]	Pins	Package Pitch (mm)	Outer Contact	Package Size (mm)	Package Thickness (mm)
Chip Scale [16,17,47]	<100	0.3–0.65	Pad	1.1 · IC	0.3 (discrete)–0.75 (IC)
EPS [46,50,51,59]	<100	0.5, 0.75, 1.0	Land	IC + 1.0	Die + 0.63
Fujitsu [18–20,56]	16–352	0.5–1.27	Lead or ball	>1.1 · IC	>0.7
GE [21,54]	<400+	Custom	Solder ball	IC	Thinned IC + flex
IBM [22]	1500	0.5	Solder ball	IC + 10	3.4
LG Semicon [23–25,133,136]	60	0.8	Lead	IC + 1.8	0.48–0.82
Matsushita [26,27,28]	100 ~ 400	0.5–1.0	Pad	IC + 4	1.6
Mitsubishi [29,30,31]	96, 256, 1024	0.5–0.8	Stacked solder ball	IC + (<0.6)	IC + 0.3
Motorola [32–34,48,55,58,172]	40–150	0.8	Solder ball	IC + (<1.5–2.5)	1.0
NEC [35]	100 ~ 1000	0.8	Solder ball	IC + (<1.0)	<1.6
Nitto Denko [36]	<100	0.5–1.0	Solder ball	IC + (<0.4)	Die + 0.35
Sandia/Aptos [37,131]	34–275	0.5–0.76	Pad or ball	IC	Die + Thin film
ShellCase [38,39]	Peripheral	>0.25	Pad	IC + 0.1	0.3–0.5
Tessera/Amkor/ Shinko elec. [40–42,52]	18 ~ 1000	0.5–1.0	Solder ball or Ni/Au bump	IC + (<1.2)	Die + (0.3–0.5)
TI Japan [4,43,49,53,57]	62–176	0.5–0.8	Solder ball	IC + 2.0	1.2
Toshiba [44,45]	100 ~ 700	0.5–0.8	Pad or ball	IC + (1–3)	1.0–1.2

Small Outline No Lead (SON), Thin Zero Outline Package (TZOP), Bottom Leaded Package (BLP), Land Grid Array (LGA), etc. [62]. Consider the LOC version depicted in Fig. 18-4 [63]. The device bond pads are moved inward towards the middle of the chip; the lead-frame terminations overlap on the device, and are attached with a 100-micron thick, double-stick adhesive tape. Electrical interconnection between the device and lead-frame is accomplished via Au-wire bonding. The asymmetric package is then overmolded with epoxy and a lead-forming operation performed to give J or C-shaped leads. A bottom leaded package (BLP) is a specific type of lead-on-chip package of which there are several variations predicated on whether the device bond pads are located at the perimeter or middle of the device, and whether the active side of the device is facing up or down. This design accommodates larger chips than are otherwise possible with a conventional design. A good choice of the molding compound is critical to preventing package warp in the asymmetrical package. Suitable modifications of the encapsulation allows these devices to be stacked as shown in Fig. 18-5 [64,65].

18.3.3 Rigid-Interposer Type

Rigid interposers provide an interconnection path between the bond pads on

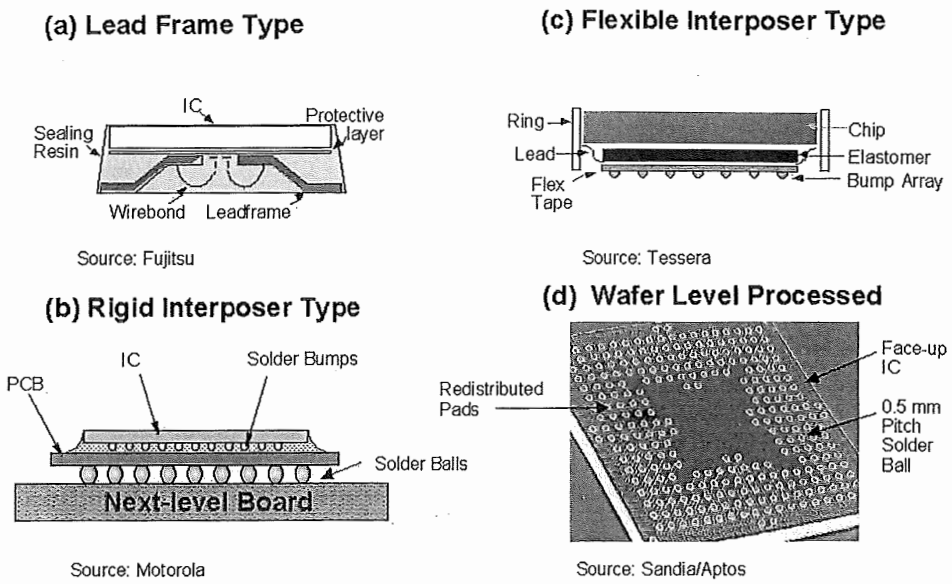


Fig. 18-3 Representations depicting the four main chip-scale package categories. (a) Lead-frame, (b) rigid interposer, (c) flexible interposer, and (d) wafer level processed.

integrated circuit devices and chip-carrier pads. They are classified in two groups, namely organic or ceramic.

18.3.3.1 Organic Standard printed wiring board (PWB) technologies are used to produce organic interposers. Process limitations currently restrict PWB construction to 3-mil lines and 3-mil spaces. Bismaleimide Triazine (BT) resin is preferred over other board materials due to its superior thermal stability compared to other common resin systems.

SLICC package. An early CSP version described by Banerjee and Lall [66] designated Slightly Larger Than IC or SLICC (Fig. 18-6), consists of an 8 to 12 mil thick rigid organic carrier, e.g., FR-4 or BT resin. The die, with 3 to 5 mil diameter, high-melt (97Pb/3Sn) solder balls on a 10-mil pitch are attached to the organic substrate with a near-eutectic solder, and epoxy underfilled for enhanced fatigue life. The board-level interconnect is accomplished with 22.2-mil diameter silver-containing, near-eutectic solder (36Pb/62Sn/2Ag) balls attached to the

Table 18-2 Manufacturers of lead frame CSPs with varying die-to-interposer and external connections

Manufacturer	Interposer	Die-to-Interposer Connection	External Connection
Fujitsu [18–20,56]	Lead frame	Wire bond (die face-down)	Lead
LG Semicon [23–25,133,136]	Lead frame	Wire bond (die face-up)	Lead
TI–Japan [49,53]	Lead frame	Wire bond (die face-down)	Solder ball
Others: Fujitsu's Bump Chip Carrier (BCC) [70], Hitachi Cable's Lead-on-Chip CSP (LOC-CSP) [70], etc.			

Table 18-3 Manufacturers of rigid interposer CSPs with varying interposer materials, and die-to-interposer and external connections

Manufacturer	Interposer	Die-to-Interposer Connection	External Connection
Matsushita [26,27,28]	Ceramic (2 to 4 layers)	Flip chip with gold stud bumps and silver-palladium adhesive	Land
Toshiba [44,45]	Ceramic (1 layer)	Flip chip with gold-gold solid phase diffusion	Land or ball
Motorola [32–34,48,55,172]	PCB	Flip chip	Solder ball
IBM [22]	Ceramic (multilayer)	Flip chip	Solder ball
Others: Amkor/Anam's Chip Array [60], EPS' NuCSP [51], IBM's FC-PBGA [70], etc.			

substrate on a 32-mil pitch. Owing to the line and space limitations of the FR-4 or BT resin printed wiring board technology, the package is limited to less than 200 I/O.

JACS package. A modified version of SLICC package utilizes a die with Sn-Pb eutectic balls and a semi-rigid glass laminate or polyimide carrier. Double-sided wiring facilitates fan-in and fan-out circuitry. This package design is termed Just About Chip Size (JACS) package [47] with several 0.8 and 0.5 mm-pitch, area-array and perimeter array configurations reported.

QFN package. An example of rigid organic interposer in a non-leaded CSP is the Quad Flat No-Lead (QFN) package depicted in Fig. 18-7. An 18-micron thick copper layer wrapped around 0.55-mm thick BT substrate is sequentially overplated with 10 μm copper, 13 μm nickel, and 0.4 μm thick gold. The copper is to define the pad terminations. The laminate outside edges are removed to prevent shorting, and then punched out to provide cylindrical surface terminations. After device attachment and wire bonding the package is encapsulated with an epoxy-molding compound. The capillary action of the semi-cylindrical terminations are

Table 18-4 Manufacturers of flexible interposer CSPs with varying interposers, and die-to-interposer and external connections

Manufacturer	Interposer	Die-to-Interposer Connection	External Connection
Tessera/Shinko/Amkor [40–42,52]	Gold/copper on polyimide flex, bonded to chip with elastomer	Thermosonic gold-aluminum bond (die face-down)	Ni-gold bump or solder ball
NEC [35]	Copper/polyimide flex, bonded to chip with polyimide adhesive	Double bump bonding (thru holes in polyimide tape) (die face-down)	Solder ball
Nitto Denko [36]	Gold/copper on polyimide flex (ASMAT), bonded to chip with TAPI*	Thermosonic gold-aluminum bond with TAPI (die face-down)	Solder ball
GE [21,54]	Copper/polyimide multilayer flex, bonded to chip with adhesive	Laser drilled vias plated with copper (die face-down)	Solder ball
Others: 3M's Enhanced Flex CSP [74,171], IZM's flex PAC [70], TI-Japan's μStar BGA [53], etc.			

TAPI: Thermo-Adhesive Polyimide

Table 18-5 Manufacturers of wafer level interposer CSPs with varying interposers, and die-to-interposer and external connections

Manufacturer	Interposer	Die-to-Interposer Connection	External Connection
Chip scale [16,17,47]	On wafer interconnect with epoxy	Gold beam lead (die face-up)	Land (silicon post)
Mitsubishi [29–31]	Copper interconnect + UBM + transferred inner solder bump + copper pad + epoxy	On chip interconnect (die face-down)	Stacked solder ball
ShellCase [38,39]	On wafer with glass plates and adhesive	Extended die pads and plated metal (die face-down)	Land
Sandia/Aptos [37,131]	Tow layers each of copper and polyimide	On chip/wafer interconnect (die face-down)	Land, gold bump or solder ball

Others: Flip Chip Technologies' Ultra CSP [81], Fujitsu's Super CSP [56], Intarsia [107,179,180], National Semiconductor's μSMD [138], etc.

intended to enhance solder joint fillet formation. The package was reported to have survived 200 thermal cycles at −40 to 85°C, a reasonable reliability for a leadless package [67].

18.3.3.2 Ceramic Ceramic interposers are heavier than laminate interposers and also have lower coefficients of thermal expansion (CTE), which make them more compatible with semiconductor dice but less compatible with conventional printed wiring boards. They can be produced with 2-mil lines and spaces to provide greater routability and hence lend themselves to CSPs requiring high wiring densities and I/O counts compared to the laminate CSPs. Figure 18-3b shows an example of this type of CSP, which is basically a flip-chip, ball grid array (FCBGA) package. However, rigid-interposer-based CSPs can also have a wire bonded die, plastic molding, and external solder balls (Fig. 18-8). Table 18-3 lists several examples of rigid-interposer-based CSPs with varying interposer materials, and die-to-interposer and external connections.

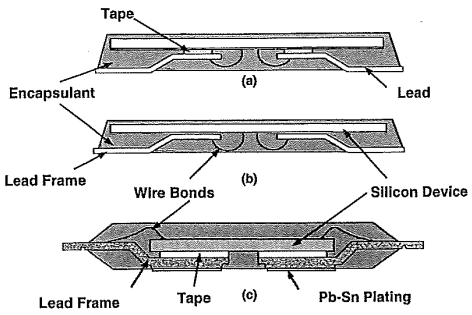


Fig. 18-4 Schematic of three bottom leaded packages (BLP). (a) Tape Lead On Chip (LOC), (b) Ultra-Thin Small Outline Non-leaded package (USON), (c) S-BLP with device facing up and perimeter IC bond pads.

Flip chip package. The IBM 21 × 21 mm ceramic mini-ball grid array package is another example of rigid-ceramic-interposer CSP that is very similar to conventional ceramic packages except for the 0.25 or 0.5-mm pitch area-array interconnections (Fig. 18-9). It consists of a multi-layer ceramic substrate with Ni/Au pad metallurgy on both sides. The flip-chip mounted device (10 × 10 mm) intended for high-speed switching [68], utilized standard high temperature (97Pb/3Sn) solder balls with 0.23 mm pitch. Decoupling capacitors are also mounted on the top side. An underfill material is used to enhance the C4-joint fatigue life and an aluminum cap is used to protect the device. In addition, the cap also serves as a heat sink for thermal management. A thermal paste is introduced between the backside of the silicon and the metal cap. The package I/O consist of 0.25-mm diameter

EX. 1004 - Page 46

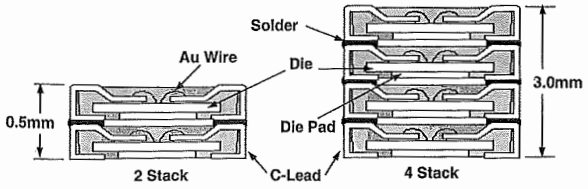


Fig. 18-5 Three dimensional packaging module (3DPM) constructed by stacking small outline C leaded (SOC) lead on chip (LOC), bottom leaded packages (BLP).

eutectic balls on a 0.5 mm pitch. Although the package does not comply with the 1.5X area CSP definition, it is smaller than standard BGA packages and so is referred to as a mini-BGA. It has high I/O capability of up to a 29 × 29 area array.

Process flows. A general process flow for the fabrication of rigid interposer CSPs is shown in Figs. 18-10 and 18-11 for wirebond and flip-chip attached die respectively. Depending upon the nature of the substrate, the device is either wire bonded or attached using flip-chip reflow. Chips are protected by either encapsulation with over-molding epoxies or a metal cap attached with glass to metal seal.

Low CTE ceramic carrier. Another example of the ceramic interposer is a Kyocera 233-I/O package. Ceramic interposer packages should be carefully evaluated within the context of product applications to ensure requisite reliability due to the CTE mismatch between the board and component. New ceramic materials with CTEs in the range of 9–11 ppm/°C are slowly coming into use [69,70]. Although this increases the CTE mismatch between a die and ceramic carrier, it serves to make the normally large CTE difference between the ceramic carrier and PCB more manageable.

18.3.4 Flexible Interposer Type

Flexible-interposer CSPs utilize a flexible substrate, e.g., flex-circuit material or tape, to provide the interconnection path between die and chip-carrier pads. Their fabrication process flow is similar to rigid-interposer CSPs (Fig. 18-10). A Tessera package (Fig. 18-12) is the most widely used flexible-interposer CSP design. Its construction consists of a polyimide tape with gold-plated copper circuitry to transfer peripheral IC bond pads to an array of solder balls located underneath the die for external connections. The flexible interposer relieves stresses induced due to the CTE mismatch between the die and the PWB [71]. Several versions are in use.

18.3.4.1 Three-layer tape version In another version, the Texas Instruments MicroStar™ BGA (Fig. 18-13), a circuitized

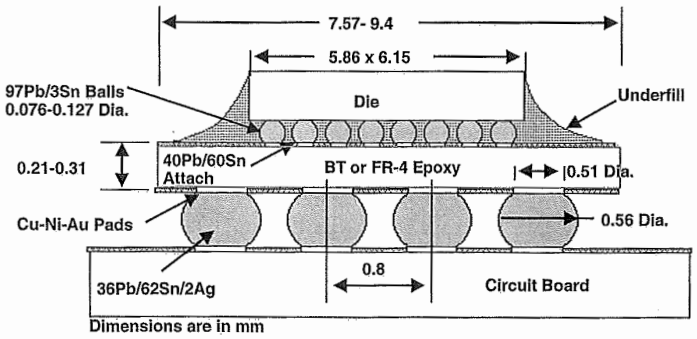


Fig. 18-6 Schematic of slightly larger than integrated circuit carrier (SLICC) package.

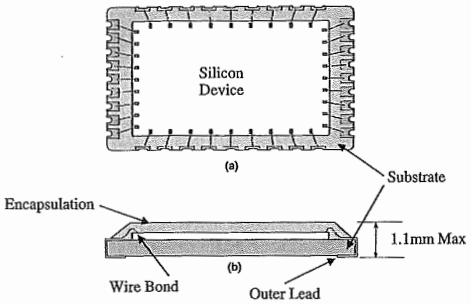


Fig. 18-7 Schematic of a quad flat no-lead (QFN) package with a wire bonded die. (a) Top view shows wire bond interconnections between perimeter die pads and mating substrate pads. (b) Side-view profile of the package.

three-layer polyimide tape is used as the interposer. Fine line (40 microns) circuitry with bond pads overplated with Ni/Au to facilitate wire bonding, is provided on the top surface. 200-micron plated vias provide the interconnection between the top and bottom layers. The device is backside bonded to the flexible interposer with nonconductive adhesive and thermosonically wire bonded to bond pads on the polyimide. It is then overmolded with an encapsulant for physical protection. Eutectic or near-eutectic solder balls are attached to the plated vias on the bottom side of the flexible interposer [72].

18.3.4.2 Enhanced flex The Enhanced Flex CSP is to provide improved electrical and thermal performance, and reliability. In this case, the interposer is a circuitized 50-micron thick polyimide tape to which a 5-mil thick patterned copper interposer is adhesively bonded. The die is adhesively attached and then thermosonically gold wire bonded to the interposer. The whole structure is overmolded with an encapsulant.

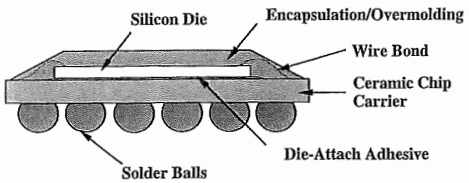


Fig. 18-8 Side-view schematic of a typical rigid interposer type CSP with a wire bonded die.

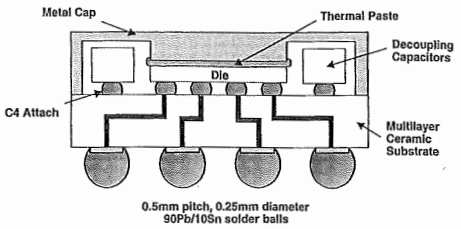


Fig. 18-9 Side-view schematic of the IBM 21 × 21 mm multilayer ceramic (MCC) rigid-interposer type mini-BGA package containing a flip-chip die and several C-4 attached decoupling capacitors. (Courtesy of IBM Corp.).

Eutectic solder balls are attached to the underside of the package for board level interconnection. Figure 18-14 shows a cross section of a Flex-CSP [73,74].

18.3.4.3 Floating pad technology An extension to the flex-interposer design concept is the floating-pad technology (FPT), which involves 25–50 micron feature polyimide structural elements. In this design a compliant micro-cup under the area-array pads isolates the package from the board; the microcup can either be air or elastomer filled. Four conductive micro beams radiate in a spiral pattern to connect the central ball mounting pad to perimeter micro-via structures that interconnect to device pads. A

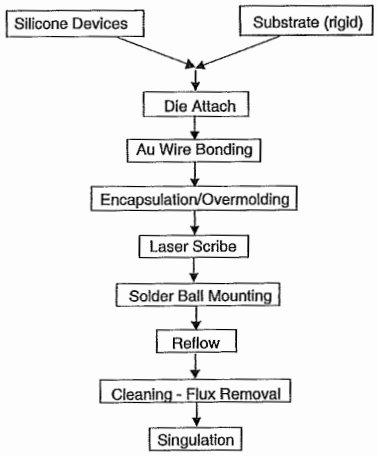


Fig. 18-10 Typical process flow for fabrication of a rigid-interposer type chip scale package with a wire bonded die.

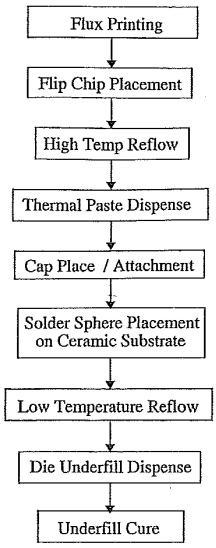


Fig. 18-11 Conventional process flow for a rigid-interposer (ceramic) type chip scale package with flip-chip die.

schematic cross-section of the floating pad structure is shown in Fig. 18-15. Several alternative structures such as S-shape, interlocking circles, etc., are possible in place of the spiral arms. A conventional ball attach process is used for mounting the solder balls. Thus, the solder-joint stress is relieved owing to the flexible nature of the structure. It was reported that this pad structure can be integrated as wafer level CSPs. It was also reported that multichip modules fabricated with air-filled micro-cups exhibited −55 to 150°C thermal cycling reliability in excess of 5000 cycles [75].

18.3.4.4 Double-sided metallized films Double-sided metallized films are also becoming available for use as interposers. They provide a significant increase in routing density and facilitate chip stacking. Currently, 50-micron lines and 40-micron spaces are used in production designs with 25-micron via diameters. The technology has the potential of producing 30-micron lines and spaces [76]. Figure 18-16 illustrates a routing scheme that allows five lines between solder pads instead of just two by utilizing an interposer metallized on both sides.

18.3.5 Wafer Level Process

In consideration of the CSP types previously described, namely custom lead, flex interposer and rigid-interposer, individual devices are attached to a lead frame or substrate structures that interconnect die pads on the device to solder terminations at the board level. Most CSPs are fabricated on an individual basis independent of the type. However, with a wafer-level process, CSPs are processed in large batches at the wafer stage. Two methods are used.

18.3.5.1 General process/construction schemes

Example A. In one case a wafer with a large number of dice and substrates is processed separately and individually tested for electrical integrity. The good packages and wafer are brought together and joined in a sequence of process steps making all the interconnections between the devices and the packages. Solder balls that enable the interconnections to the PWB are then attached to the wafer assembly and then the packages are singulated (i.e., divided into individual packages). Figure 18-17 shows a wafer-level

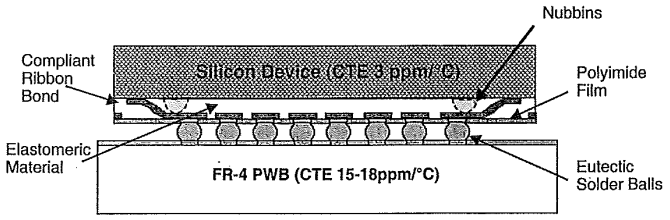


Fig. 18-12 Schematic of flexible interposer chip scale package with ribbon bond. Compliant (flexible) interposer relieves CTE-mismatch induced stresses between die and organic carrier.

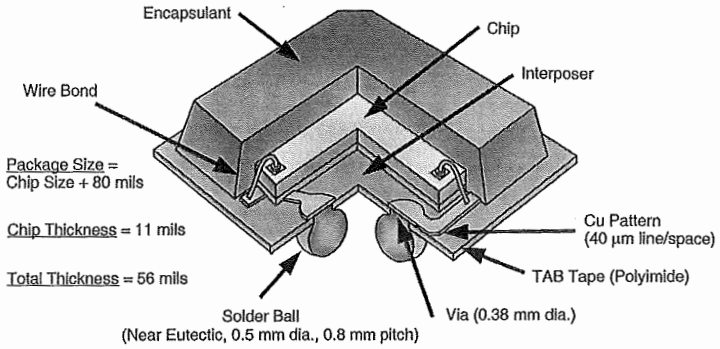


Fig. 18-13 Drawing of TI Japan's Micro Star BGA™. (Courtesy of Texas Instruments).

process flow for the fabrication of the chip scale packages [77]. Several process variations are in vogue depending on the fabricator and material sets involved.

Example B. In a second case the wafer is processed in a manner that is integral to a wafer after electrical test. For example, the wafer is spin coated with a first dielectric layer and then the vias are patterned and etched to expose the die bond pads. Then the barrier metals (Ti/W) and seed (Cu) metallurgies are sputtered. Subsequently, the wafer is patterned and the interconnection metallurgies (Cu, Ni) are plated. The barrier and seed metals are etched and a second dielectric coating is applied. Vias are then patterned and etched to define solder-bond pads on the interconnect metal. Barrier and seed materials are again sputtered, followed by patterning and plating of interconnect metallurgies, namely Cu and Sn/Pb solder. Finally, the barrier and seed metals are etched and the plated solder is reflowed to form solder balls for board-level interconnections. After the wafer-level processing the wafer is singulated to yield individual packages. Wafer-level packaging is adaptable to both perimeter and area-array pads on a chip [37,78].

Example C. In yet another wafer level fabrication scheme, a layer of polyimide is first deposited on the wafer passivation layer and Ti/Ni metallurgy deposited on the aluminum pads providing a first-level interconnection. Copper traces and bond pads are patterned using photolithography in a manner that allows the peripheral I/O on a device to be redistributed to the package area array I/O. Thick copper of approximately 90 μm on under bump metallurgy of nickel, and solder are sequentially plated on the redistribution

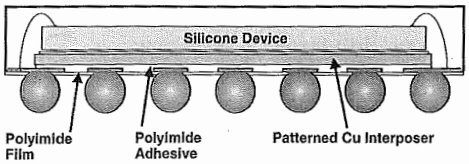


Fig. 18-14 Cross sectional schematic of an enhanced, flex based, cavity up, CSP. A patterned copper interposer improves thermal performance and improved CTE matching with circuit board.

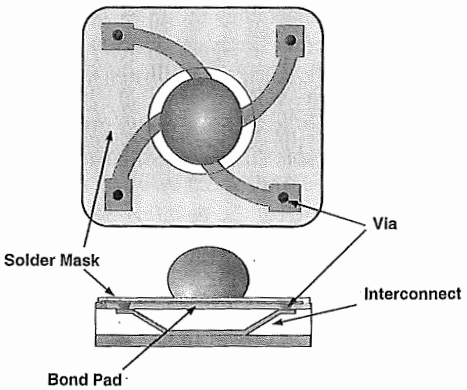


Fig. 18-15 Schematic of a flexible interposer CSP that utilizes a floating pad technology to significantly enhance the board-level solder joint fatigue life. (a) Top view. (b) Cross section of package construction.

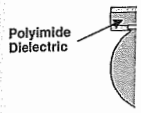


Fig. 18-16 S
enhanced rou
ble interposer
Sheldahl [76].

bond pads.
capsulation
lation and e
the under bu

18.3.5.2 l
packages ut
18-18) syste
The first la
plied to the
provide a pa
Al/Ni/Cu is
stitute trace
A second I
provide pas
and definiti
subsequent
lapped if ne
microns) ar
gulated to

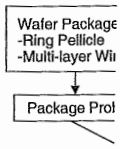


Fig. 18-17
level chip s

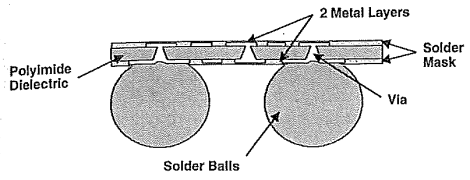


Fig. 18-16 Schematic illustrating a significantly enhanced routing capability by utilizing a flexible interposer metallized on both sides. (Source, Sheldahl [76]).

bond pads. The process is completed by encapsulation with a molding compound, singulation and eutectic solder ball attachment to the under bump metallurgy (UBM) [79,80].

18.3.5.2 Ultra CSP So-called Ultra-CSP packages utilize a two-layer dielectric (Fig. 18-18) system of benzocyclobutene (BCB). The first layer of BCB (10 microns) is applied to the device, exposed and developed to provide a passivation and planarization layer. Al/Ni/Cu is then sputtered and etched to constitute traces and an under bump metallurgy. A second BCB layer is similarly applied to provide passivation and redistribution wiring and definition of the solderable areas for the subsequent ball attachment. The CSP is then lapped if necessary and solder balls (250–450 microns) are attached. The wafer is then singulated to yield individual devices [81,82].

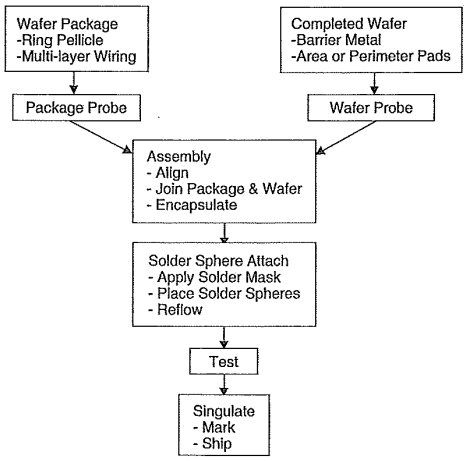


Fig. 18-17 Manufacturing process flow for wafer-level chip scale package fabrication.

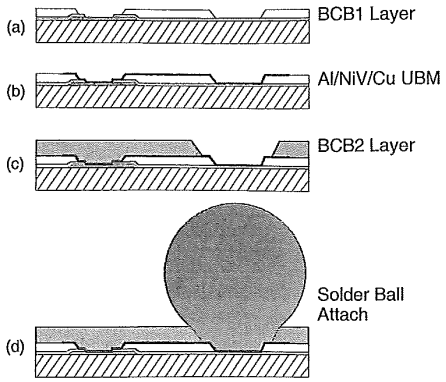


Fig. 18-18 Schematic representation of the fabrication sequence for Ultra CSP construction.

18.3.5.3 WAVE technology Another wafer-level packaging technology is called Wide Area Vertical Expansion (WAVE) technology [83] and provides circuit interconnection at the wafer level. An interposer layer is created and attached to the wafer in a mass joining process. Interconnection between the die and circuit interposer is accomplished through "compliant vertical links" or S-shaped Cu wires. After attachment, the assembly is expanded vertically and a low modulus encapsulant is injected into the cavity. Solder balls are then attached on the bottom side, followed by test, burn-in, and singulation. The compliant layer and Cu leads are to provide increased stress relief to compensate for the CTE mismatch between the die and circuit board for enhanced solder-joint life.

18.3.5.4 Enhanced BCC packages Chip scale package technology is still evolving and maturing. For example there is an effort underway to eliminate interposers altogether and the concept is called Bump Chip Carrier (BCC) and enhanced Bump Chip Carrier (BCC^{++}). These are interposerless technologies.

Bump Chip Carrier CSP design was designed for radio frequency communication [84]. This design does not use an interposer (Fig. 18-19); instead a copper lead frame material is etched out to form lead terminations and cavities for the semiconductor device. The etched concave surfaces are sequentially

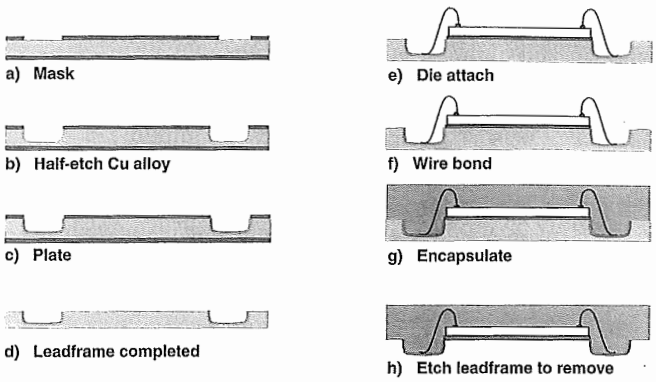


Fig. 18-19 Schematic of the process flow for the fabrication of Bump Chip Carrier (BCC) chip scale packages.

plated with Au (50 A), Pd (0.1 micron), Ni (0.5 micron), and Pd (0.5 micon) metallurgies. These metallurgies provide relevant surfaces for wire bonding, diffusion barrier, die attachment, and solderability. The die is mounted in the central cavity with a silver paste, then connected to the terminals and the brim for grounding with Au wire bonds. Gold stud bumps bonded to the terminals provide adequate strength. The lead frame with the wire bonded device is overmolded with a suitable epoxy. The lead frame is then etched out using the plated metal as a resist. The overmolded wafer is singulated to yield discrete packages. The plated bumps/studs act as the interconnection medium to the printed wiring board. This interposer-less construction combined with a high filler content (90%) biphenyl epoxy mold compound was reported to provide a thermal cycling reliability of 1200 cycles at −65 to 125°C [85]. Since conventional high volume PWB manufacturing processes are used this package is considered to be very cost effective. Typical applications include phase-locked loop synthesizers.

18.3.5.5 Commercially-available CSPs

Several wafer-level redistribution chip scale packages are available in the industry. These include Chip Scale's micro-SMT, EPIC's chip scale package, Fujitsu's super CSP, Mitsubishi's CSP, National Semiconductor's microSMD, Sandia Laboratories' miniBGA (Fig. 18-20), Shellcase's ShellPACK/ShellBGA [86], and many others.

18.3.6 Comparison of CSP Designs

The four major types of CSP approaches are summarized in Table 18-6, with each CSP approach having its own advantages and disadvantages. Lead-frame-based CSPs have the advantage of a relatively mature infrastructure, but are basically a solution for ICs with low pin counts, usually less than 50. Rigid interposer-based CSPs evolved mainly from conventional BGA packages and usually have the largest foot prints among the four CSP approaches. Flexible-interposer-based CSPs are among the most popular and recognized type. However, the manufacturing cost associated with their relatively complicated structure is a key factor as to whether flexible-interposer CSPs will eventually become the mainstream CSP approach. Each CSP structure must be carefully evaluated in terms of the board structure, surface finish, and environmental requirements for each application.

18.4 CSP Board-Related Issues

18.4.1 Standardization and Availability

Manufacturable CSP components must conform to several design specifications. The

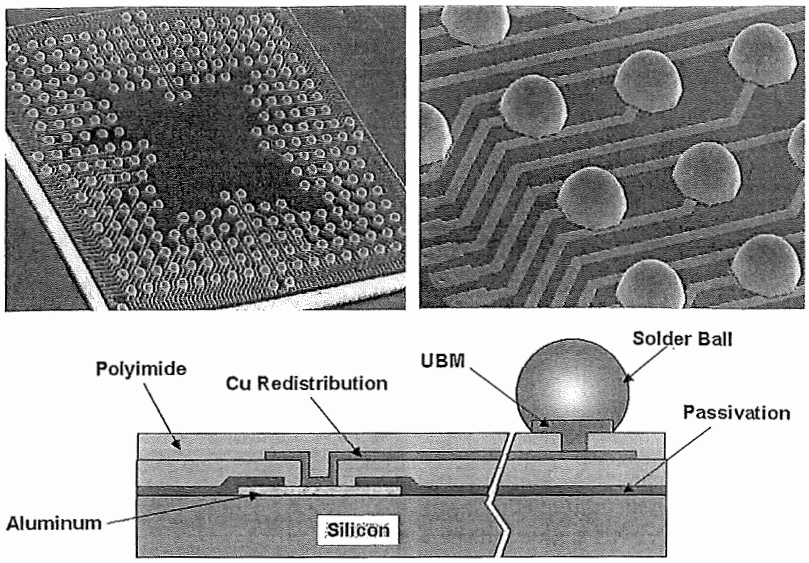


Fig. 18-20 An example of on die/wafer pad redistribution. The figure shows a miniBGA made for Sandia by Aptos. The die is approximately 10 mm (0.4″) square with 275 redistributed pads at a solder ball pitch of 0.5 mm (0.020″). The upper left of the figure shows the top view of the die with redistributed pads, the upper right shows an enlarged view of one die corner, and the lower part illustrates the cross section of the redistributed die (or miniBGA). The symbol of UBM stands for under bump metallurgy.

J-Std-012 noted earlier [13,47,87] is by no means complete, but does detail such things as shipping and handling methods, containers, test and burn-in requirements, while component size and thickness remain to be standardized and specified. Some effort has been made to standardize the package outlines by the JEDEC JC-11 committee. JEDEC publication 95 and EIA publication PDP-100 list recommended package outlines and tolerances [88]. Reference to supplier drawings is also recommended as deviations from the JEDEC dimensions do occur [89].

Table 18-6 Comparison of the most common CSP design approaches

Criteria	Lead Frame	Rigid Interposer	Flexible Interposer	Wafer Level Processed
I/O type	Periphery	Array or periphery	Array or periphery	Array or periphery
Pin count	Low	Medium to high	Low to medium	Low to medium
Footprint (pkg/chip)	1.0 to 2.0	>1.2 X	< or >1.2 X	~1.0 X
Typical thickness (mm)	09 to 1.5	1.0 to 2.0	0.8 to 1.2	0.3 to 1.0
Outer lead/ball pitch (mm)	0.4 to 0.65	0.5 to 1.0	0.5 to 1.0	0.2 to 0.8
Infrastructure	Good	Some	Limited	Limited
Estimated $	Low to medium	Medium	Medium to high	Low to medium
Production (as of 4/99)	Some	Minimum	Some	Least

18.4.1.1 Die shrink considerations Adherence to standard package outlines can help address die shrink and obsolescence issues. Semi-conductor manufacturers are continually refining and enhancing their processes to improve wafer yields. Reducing feature size allows an increase in the number of die for a given wafer area. As this occurs the original die size may no longer be available, so a package must be designed to accommodate die shrinks without requiring a board redesign.

18.4.2 Board CTE

High-reliability applications often expose a card assembly to challenging temperature conditions combined with severe mechanical stresses. Key among design concerns are the solder-joint strains induced due to the coefficient of thermal expansion (CTE) mismatches between components and the printed wiring board. Coefficient of thermal expansion mismatches greater than 4 or 5 ppm/°C can limit the reliability of the assembly. The situation is aggravated by direct die attachment to the PCBs, ceramic chip carriers, increased footprints, larger die, and greater thermal excursions. Methods for reducing the board CTE include the incorporation of Kevlar® fibers, adding ceramic fillers into the board materials, and embedding low CTE metals such as copper/invar/copper (CIC) foils at various layers within a board. For example, using metals with CTE near 5 ppm/°C in combination with board materials where CTEs are near 20 ppm/°C can reduce the global CTE of a board to a range of 9 to 11 ppm/°C.

18.4.3 CTE—Compensated Boards

Use of embedded low CTE materials can create internal stresses within a PCB. Surface preparation and adhesive selection are critical steps in the board fabrication and must be well addressed to prevent premature layer separation within the PCB. Vendors experienced with producing these boards should be consulted to avoid application errors. As an example Fig. 18-21 shows a board delamination which resulted from a poor bond to low CTE materials under an area-array package. Passing the board through the 210°C reflow temperatures was sufficient to cause the internal layer separation. The resulting bulge in the board caused opens on one side of the area array component. The delamination was not due to popcorning as proper drying and handling procedures were observed.

18.4.4 Solder Mask Issues

For area-array package assembly there are two prevalent solder mask configurations on land pad designs that are employed

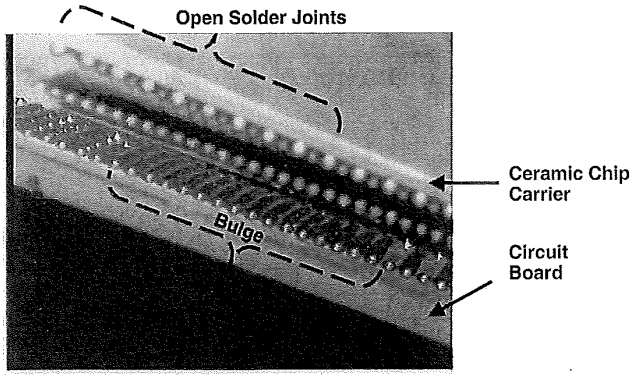


Fig. 18-21 Photograph of a delamination due to poor bond strength of board layers to low CTE materials built into the circuit board laminate. The resulting bulge lifted one end of the fine pitch ceramic area-array chip carrier (background) off the board during first pass reflow.

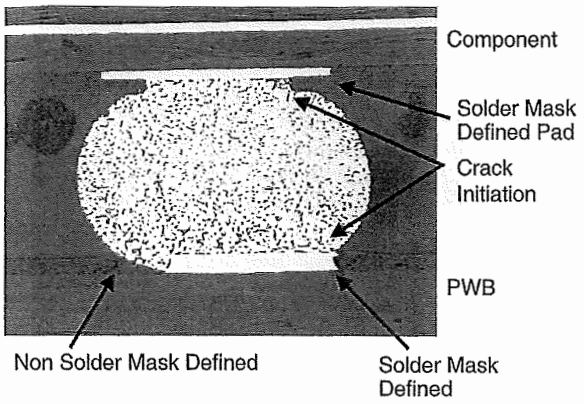


Fig. 18-22 Example of partial solder mask defined pad due to poor solder mask registration. Crack initiation typically occurs at solder mask contact area.

throughout the industry, namely, solder-mask defined (SMD) and non-solder mask defined (NSMD) lands. SMD and NSMD pad designs can be used with any shape land pad, round pads being the most common. In terms of preferences there are those that believe both designs to be acceptable and those that strongly advocate non-solder mask defined pads for better thermal cycling reliability [90]. The choice of pad designs primarily depends on the product design, application environment, the package pitch, PWB materials, and budgeted fabrication costs.

18.4.4.1 Solder mask defined pad (SMD) With SMD land pads, the underlying copper pad is larger than the opening in the solder mask. Pad dimensions are defined by the opening in the solder mask and its positional accuracy is influenced by solder mask registration tolerances. Also, copper pad adhesion may be slightly better due to the overlapping solder mask. Advocates of SMD pads claim an increased solder-joint height resulting in improved reliability of the solder joints versus NSMD solder joints [90]. However, the intersection of the solder and the mask provides a high stress region where initiation of fatigue cracks is likely to occur during thermal cycling.

18.4.4.2 Non-solder mask defined pad (NSMD) NSMD pads are isolated from the solder mask by an annular ring and defined only by the design and the copper-etch characteristics. Typical annular rings or solder mask openings provide a clearance between the land pad and the edge of the solder mask of approximately 0.06 mm (2.5 mils). Good registration of the solder mask is important and a consistent 1 to 2-mil wide clearance ring between the mounting pad and the mask edge is desired. Poor solder mask registration can cause partial solder mask defined pads, which leads to early crack initiation and propagation at the point of contact between the solder mask and the solder joint during thermal cycle conditions (Fig. 18-22). Annular rings with less clearance can also restrict uniform formation of solder around the edge of a land pad. One study has shown this condition to contribute to the formation of cracks in the laminate [91]. Advocates of NSMD pads claim the stress concentrations where the edge of the solder mask and a solder joint make contact is aggravated by the z-axis expansion of the solder mask during thermal cycling, resulting in lower reliability. For detailed discussion of solder masks and their effect on reliability see Chapters 19 and 18 respectively.

For a 0.76-mm pitch package assembly a 0.30-mm (12-mil) diameter pad is generally used. For a SMD pad, if the solder mask overlaps on the pad by 1 mil, the actual copper land will be 14 mils. That leaves 16-mil space between the pads. This implies it can accommodate one 5.3-mil line with 5.3-mil space per

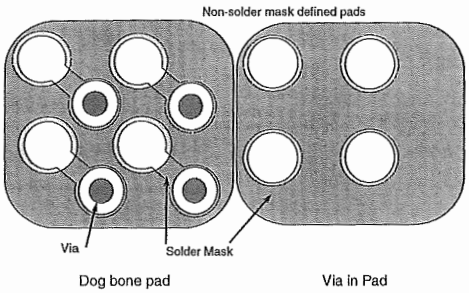


Fig. 18-23 Illustrated top view of dogbone and via in pad designs.

channel. On the other hand if one chooses a NSMD pad, a 12 mil pad provides 18-mil space between the pads and allows a one 6-mil line with 6-mil space per channel. Five mil to 6 mil lines and spaces are common in the PWB industry.

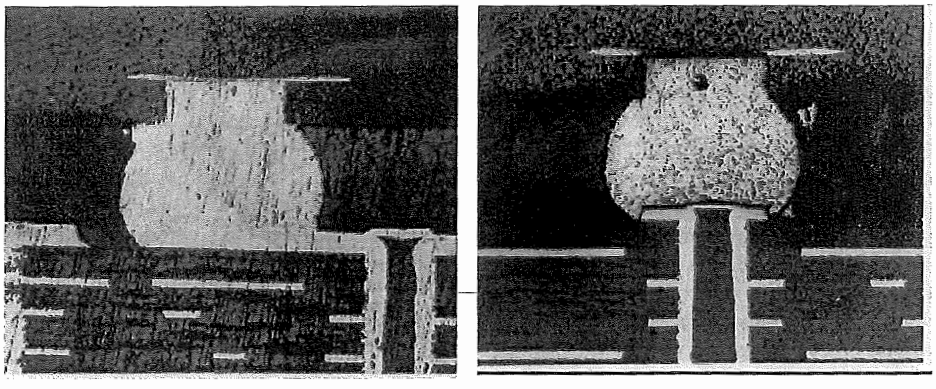
18.4.5 Mounting Pad Design

Two types of mounting pad designs are commonly used, namely the dogbone pad and via-in-pad. Dog-bone traces or via-in-pad board constructions (Fig. 18-23) can use either the SMD or NSMD configurations. Dog-bone describes offset via and land pads joined together by a trace while via-in-pad designs place filled vias directly in the land pad. Via-in-pad designs shorten the signal routing, improve thermal transfer, and allow for increased pad diameters or increased signal routing density, but are typically much more costly than dogbone designs.

Figure 18-24 shows a cross sectional view of each pad design. In these examples the vias were filled with adhesive and plated over with Cu. Filling and overplating of vias is a required step for via-in-pad. Unfilled blind vias are associated with the risk of increased voiding, solder scavenging into the via and the effects of expanding gasses during reflow. Open vias allow the solder to pass through the board and exit through the back side of the via resulting in unpredictable solder volume in the joints, voiding, and low component stand-off height (Fig. 18-25).

18.4.6 Build-up Technology

Migrating to smaller pitch components requires finer lines and spaces, and smaller vias are required than are possible with conventional PWB fabrication technology. It is possible to drill 8-mil diameter holes in thin boards (less than 40 mils thick) utilizing conventional technologies, but with reduced yields. However, industry is moving toward adopting emerging technologies variously called Surface Laminar Circuitry (SLC), Micro Via technology, Build-up



a) b)

Fig. 18-24 Cross section of two pad designs. Dogbone (a) shows the offset solder joint connected to the via. (b) One type of via in pad construction. In this example the vias were filled with epoxy, planarized, and plated over with Cu.

Fig. 18-25 V
via barrel plat
through the o
the solder joi

multi-layer t
(RDL) tech
produced b
laser, photo
With these
place to pr
pads, 4-mil
ers, and 5-n
lines and sp
the nomina
eter, via si
for several
discussion
board-level

Table

| Pit
mm (|
|---|
| 1.27 |
| 1.00 |
| 0.80 |
| 0.76 |
| 0.50 |
| 0.40 |
| 0.30 |
| 0.25 |

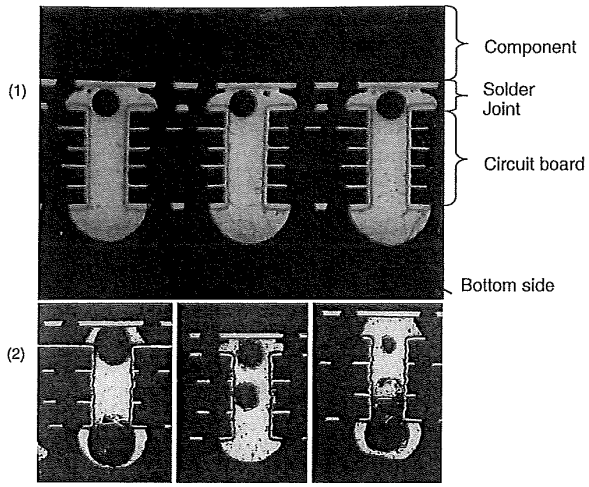


Fig. 18-25 Voiding in area array solder joints with through hole via-in-pad system, (1) with normal via barrel plating quality, (2) with poor via barrel plating quality. All examples show that solder flowed through the open vias, accumulating on the bottom side of the circuit board resulting in a reduction of the solder joint height. (Photo courtesy of Ning-Cheng Lee, Indium Corp.).

multi-layer technology, Redistribution Layer (RDL) technology, ALIVH, etc. Vias are produced by non-mechanical means such as laser, photo-defined, or plasma techniques. With these techniques it will be common place to produce 5-mil vias on 10 or 12-mil pads, 4-mil lines and spaces on external layers, and 5-mil vias on 14-mil pads, and 3-mil lines and spaces [92,93]. Table 18-7 provides the nominal dimensions, for the pad diameter, via size, line widths and spaces, etc., for several foot print pitches. For a detailed discussion of build-up technology to increase board-level densification, see Chapter 7.

18.4.7 Surface Finish

Surface finish must be considered at the time of component selection. Different combinations of solder ball metallurgy and board surface finish may require modifications of the component-attach reflow conditions using eutectic Sn/Pb solders. Difficulties with incompatibilities may result with the introduction of lead-free solders.

18.4.7.1 Solder joint embrittlement Brittle intermetallic growth associated with increased weight percent of Au and Ag in Sn/Pb

Table 18-7 Typical circuit board dimensions for CSPs with various footprints

Pitch mm (mils)	Pad Diameter mm (mils)	Via Diameter mm (mils)	Line Width mm (mils)	Line Space mm (mils)	Recommended Board Technology
1.27 (50)	0.66 (26)	0.45 (18)	0.15 (6)	0.15 (6)	Conventional
1.00 (40)	0.50 (20)	0.35 (14)	0.15 (6)	0.15 (6)	Conventional
0.80 (32)	0.40 (16)	0.28 (11)	0.127 (5)	0.127 (5)	Conventional
0.76 (30)	0.38 (15)	0.20 (8)	0.127 (5)	0.127 (5)	Conventional
0.50 (20)	0.28 (11)	0.15 (6)	0.10 (4)	0.10 (4)	Micro via board
0.40 (16)	0.23 (9)	0.10 (4)	0.075 (3)	0.075 (3)	Micro via board
0.30 (12)	0.178 (7)	0.075 (3)	0.075 (3)	0.075 (3)	Micro via board
0.25 (10)	0.125 (5)	0.05 (2)	0.075 (3)	0.075 (3)	Micro via board

solders is well documented in industry [94]. The increased weight percent of Au and Ag in the solder joints is often the result of excess plating thickness on the surface finish of the board. The condition can be aggravated when these metals are also contained in component solder spheres.

18.4.7.2 Reflow profile modification Surface finish may require modification of the solder-attachment reflow profile. For example, it has been reported that palladium finishes require longer dwells above the reflow temperature and an increase of the peak reflow temperatures [95]. Lead-free solders under consideration may require new board finishes and peak reflow temperatures of 245°C or higher in order to form the most consistent and reliable solder joints [96]. Modifications to reflow profiles utilized throughout the industry for standard eutectic Sn/Pb (220°C peak, 60 to 90 seconds dwell time) which result in an increased peak temperature or dwell time can have significant board and component reliability implications. Choice of the surface finish and the component metallurgy must be made with due considerations to the effects on the assembly processes, other temperature sensitive components on the assembly, and the board level reliability.

18.4.7.3 Pressure contacts Another consideration is the selection of a surface finish for the use of spring contacts in the assembly. These contacts typically require a Ni/Au interface. Selective plating of the spring contact areas with the Ni/Au finish and using another finish on the rest of the board can solve many other problems but will increase the board cost. Another issue with selective plating is finding a board vendor that will offer this option.

18.5 Pre-Assembly Issues

18.5.1 Board Moisture

Cycle time reduction is a key element to reduce production costs. Developing a strategy with vendors to protect circuit boards from moisture exposure and contamination can eliminate hours of cycle time. Receiving low-moisture content boards and providing low-moisture storage can eliminate the need for drying prior to reflow, significantly reducing cycle time. However, drying should always be conducted if in doubt as to the board exposure to moisture. The drying cycle depends on the board material, thickness and outside dimensions but is typically about 4 hours at 120°C. Dry boards should be protected from moisture reabsorption until just prior to assembly.

18.5.1.1 Moisture removal Chip scale packages usually are not hermetic and the moisture sensitivity level must be noted. Out-of-package life or outlife must be tracked to prevent popcorning and package delamination during the board-level assembly reflow. Moisture sensitivity typically increases with die size. Components should be packaged and labelled according to EIA/JEP113 and handled per J-STD-020, Class 1 to 6—(Classification 1, not moisture sensitive, to 6, very sensitive). Any components, which exceed their specified outlife, require a bake cycle of 125°C for 24 hours prior to exposure to a reflow process. Components packaged in tape and reel format require 192 hours at 40°C. Even with the lower temperature, cover tape adhesion can be adversely affected. Proper packaging and repackaging procedures can eliminate the need for drying cycles. Implementation of an aggressive dry-storage policy using desiccated moisture-barrier bags is strongly advised whenever possible.

18.5.2 PWB Inspection

A sample of the circuit boards should be inspected well in advance of the planned assembly date. Discovering a board problem at or after assembly is costly in terms of time, lost production, required rework and in some cases, reduced reliability. Solder masks should be inspected for registration and pad clearances, thickness, and

sufficient dam width over dogbone traces. Board surface finish should be checked for solder wettablity and the presence of defects such as "black pads" on the Ni/Au finishes (Section 18.8.4.2).

18.5.2.1 Planarity The highest probability of successful assembly for all package types occurs with flat boards so maintaining planarity is a major assembly factor. Designing boards with layer pairs produces a balanced lay up which is extremely important in preventing board warp. Every effort should be made to acquire boards with as little warp as possible. Current standards allow .0075 inches of warp per inch [97]. This is generally not a problem with CSPs given their small size, but is of increasing concern as I/O and package outlines increase.

Warp related problems. Board warp often reaches maximum displacement during reflow. This can be a source of intermittent open solder joints. In these cases an assembly enters the cooling zone after reflow and an open solder joint begins to solidify before the board is sufficiently cooled to reduce the warping. As the board continues to cool and flatten out the solidified solder joint makes contact and rounded surfaces become deformed or flattened. The resulting solder-joint shape and volume are essentially the same as "good" solder joints but metallurgical bond may not have formed. If undetected, the joint acts as an intermittent fail in the field. Evaluation of board warp immediately after exiting the reflow oven should be included as part of a reflow-profile and new job set-up procedure.

18.5.3 Component Inspection

18.5.3.1 Missing solder balls A sample inspection of components should be part of an incoming inspection plan. Any missing solder balls are an indication of a package shipping or fabrication problem. When properly attached to a package, a reasonable amount of force is required to remove the solder balls. Causes of missing solder balls include non-wettable pads, poor pad/board adhesion, mechanical damage, oxidized solder ball surface, and/or mere absence of ball in that location. Figure 18-26 shows examples of "missing" solder balls that separated from a component (a) between the pad and solder ball and (b) between the component and pad. It is prudent to obtain shear strength data for a package lot with missing solder balls as it can be related to a component quality issue. Shear test data alone may not identify all issues but can give early indications of a problem (see Section 18.8.4.2).

18.5.3.2 Debris It is important to examine the packages for contamination in the form of metallic or non-metallic particles embedded in or on the surface (Fig. 18-27), fibers, etc. Debris found on packages does not

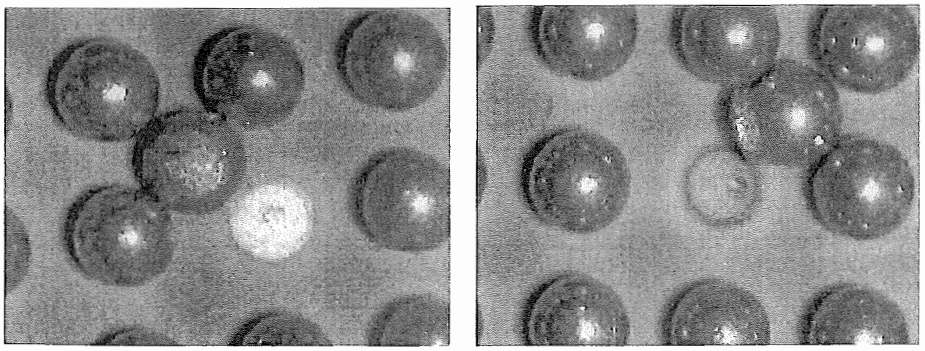


Fig. 18-26 Photographs of solder ball separations. (a) Solder ball separated from the pad and (b) pad separated from the ceramic chip carrier.

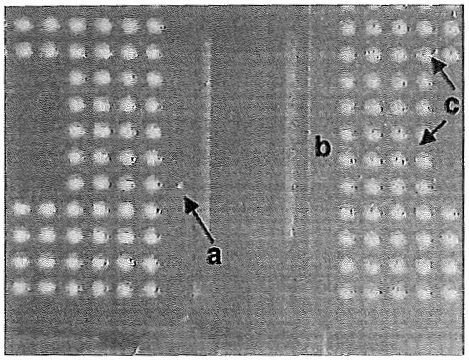


Fig. 18-27 Photograph of typical debris sometimes found on area-array packages. (a) Embedded metal particle, (b) dust from singulation, and (c) lint. These pose a greater concern with chip scale packages owing to their finer pitch.

necessarily cause failures [91]. The potential for contamination causing a problem depends on the type of the contamination, package ball pitch, and the assembly process. But the migration to finer pitch area-array will aggravate the problem. As an example, a hydrophilic fiber, which is common contaminant, in contact with adjacent balls or joints can cause an electrical short or reduce surface insulation resistance to an unacceptable value, or can cause corrosion or electromigration in high-humidity environments.

18.5.4 Component Handling/Storage

Although CSPs are much easier to handle than leaded components, they are not immune to handling damage. The ductility of Pb/Sn alloys requires that properly dimensioned matrix trays be used for those CSPs not available in tape and reel format. Additional cover trays should be acquired for low-volume operations to prevent damage when only a portion of the components in stock are delivered to the line. Components returned to storage or those issued to the line have a greater risk for damage if they do not have a cover tray.

Corner solder balls have the highest potential for damage which typically occurs by deforming the soft solder balls (Fig. 18-28).

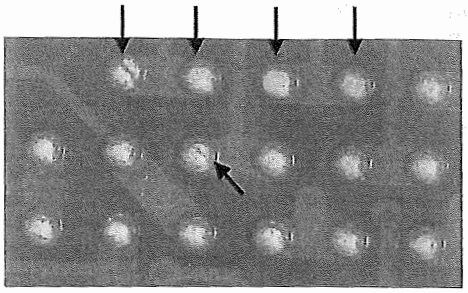


Fig. 18-28 Photograph of a portion of a CSP solder ball array showing deformed and flattened solder balls resulting from improper handling.

Damaged solder balls can cause multiple problems by exaggerating planarity-related assembly issues, and lead to high rejection rates or errors at placement and poor assembly yields.

18.6 CSP-to-Board Assembly

The usual CSP outer lead/ball pitch is not less than 0.5 mm, which avoids some board assembly problems associated with fine-pitch surface mount components. However, problems arise because CSPs are usually assembled with other components as shown in Fig. 18-29. The difference in heat capacity between CSPs and other components can make the reflow process challenging, not to mention the inspection of solder joints, cleaning, and rework. Other assembly-related issues include solder-volume specification and control, chip-carrier pad shape and size, solder mask defined versus non-solder mask defined pad [5,40,41,98–103], and solder ball height. A typical CSP solder-joint cross-section with dimensions is shown in Fig. 18-30. It is possible to manufacture robust CSP assemblies by following appropriate procedures during the assembly process [62,104,105].

18.6.1 Circuit Card Assembly Process Flow

A typical board-assembly-process flow for a printed circuit board (PCB) mounted with CSPs and conventional surface-mount

EX. 1004 - Page 60

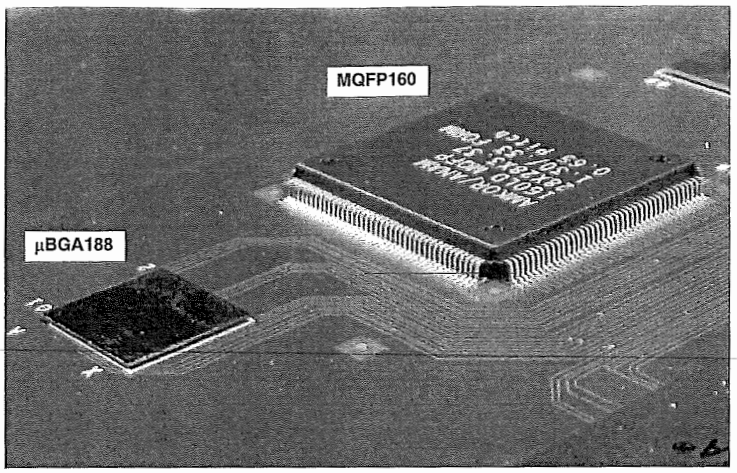


Fig. 18-29 Photograph which shows the significant difference in size, and mounting height of a CSP compared to a QFP and demonstrates the joint inspection limitations. Significant differences in thermal mass present process challenges for reflow attach of different types of components on the same assembly.

components consists of the following steps: Bake or dry the boards as required, screen print, paste inspection, pick and place (for passive devices or components with larger lead or ball pitch), fine pitch pick and place (for finer pitch components), reflow, clean (optional), test, and rework. It should be noted that as with leaded components, the accuracy requirements will increase for the pick and place equipment as pitch decreases.

One of the key selling points of the CSP is that the chip-scale components do not require the higher level of cleanliness, care in handling, and bare-die issues faced when using chip-and-wire or flip-chip die. CSPs can be assembled using conventional screen print

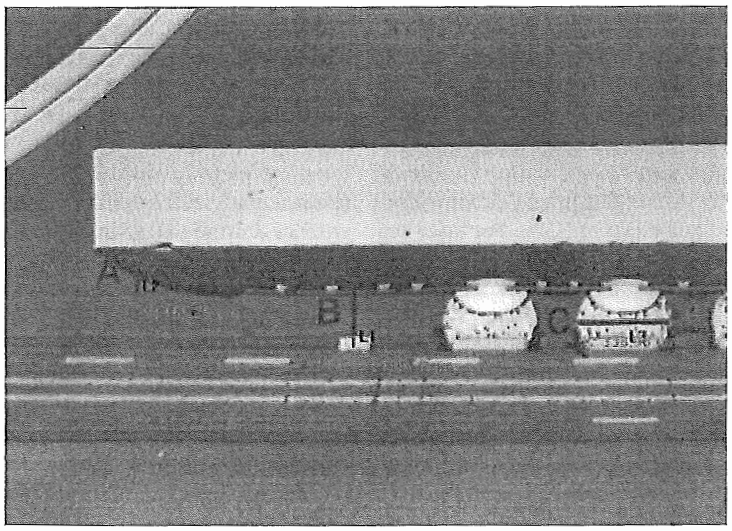


Fig. 18-30 Vertical cross section of a typical CSP solder joint with the indicated measurements of A = 160 μm, B = 190 μm, and C = 340 μm.

and pick and place equipment using tape and reel formats.

18.6.2 Stencil Design for Paste Printing

Typical CSP pitches are 0.8 mm, 0.75 mm, and 0.5 mm. These can be printed using conventional screen print equipment and very often without modification to the process used for BGAs, QFPs, and other surface mount components. Solder paste pad diameters decrease proportionately as the pitch decreases and can lead to solder paste print defects. Limits of the solder paste/stencil combinations are often evidenced by an increase in defects such as insufficient or inconsistent solder volume on the pads, conically shaped solder bricks, pullouts, and/or rapid clogging of the stencil apertures for the finer pitch components. An assembly using exclusively CSPs would be preferred. It is likely that solder volume requirements for larger surface-mount components will require the use of a 0.203 mm (.008″) or 0.15 mm (.006″) stencil.

18.6.2.1 Area ratio An effective stencil design tool that can provide an indication of the release properties is the area ratio (AR). The total wall area divides the area of the designed aperture opening. An AR greater than 0.5 was reported to provide good stencil release and uniform solder paste height. The technique works well with round or rectangular apertures [106,107].

18.6.2.2 Aperture ratio In a vast majority of cases 0.005″ to 0.006″ stencils, either chemically etched and electropolished or laser cut stainless steel with 1:1 pad to aperture ratio are employed with success for assemblies using CSPs with pitches from 1.0 mm down to 0.75 mm [91]. As the pitch decreases from 1.0 mm to 0.75 mm pull out and conical shaped solder bricks become more common. Figure 18-31 shows the solder print for different pitch components on the same board using a .006″ stencil with 1:1 apertures. It demonstrates one of the problems that can occur when coarse and fine pitch CSPs are combined on the same assembly. Thinner stencils are required to optimize print quality for the fine pitch CSPs, but the thinner stencils reduce the solder volume printed for the coarse pitch components. Maximizing the solder volume increases the reliability of the CSP components [108] and any modifications that reduce the solder volume should be carefully considered in terms of product reliability requirements before implementation.

18.6.2.3 Apertures Square apertures with rounded corners, in combination with trapezoidal openings, are often recommended for area-array components with pitches of 0.8 mm or less [109]. Paste release from apertures with this geometry is greatly improved over round apertures on fine-pitch components. Paste volume is increased for higher reliability, and the additional paste compensates for a lack of coplanarity that can be present on components. Some disadvantages can be an increase in stray solder balls found under components and a slightly greater potential for bridging. Due to the low stand off height of many CSPs, cleaning can be difficult and a no-clean flux may be preferred to hold stray solder balls in place.

18.6.2.4 Step downs The part mix complexity on the board must also be considered in the decision to make any adjustments to the stencil design. For example, populating cards with components having a wide range of pitches may require the use of step-down stencils for fine-pitch printing. Modifications to stencils in the form of step downs have been successfully used but cause some inconsistencies in solder-volume in transition areas. For example a 0.15 mm thick stencil could have a 0.102 mm or 0.127 mm thick step down for 0.5 mm pitch components. Components requiring higher volumes of solder may receive inadequate solder when fine pitch CSPs are located nearby on an assembly.

18.6.3 Solder Paste

Type 3 (−325 to 500 mesh) solder paste with 20 to 45 microns (diameter) solder particles has been demonstrated to be sufficient



Fig. 18· (a) 1.0 r a 0.006- the sam for bo: pitche: solder· print p to .00: consis Type 3 ber of Type cles p paste, der v dropi new p and r is im· cle si area

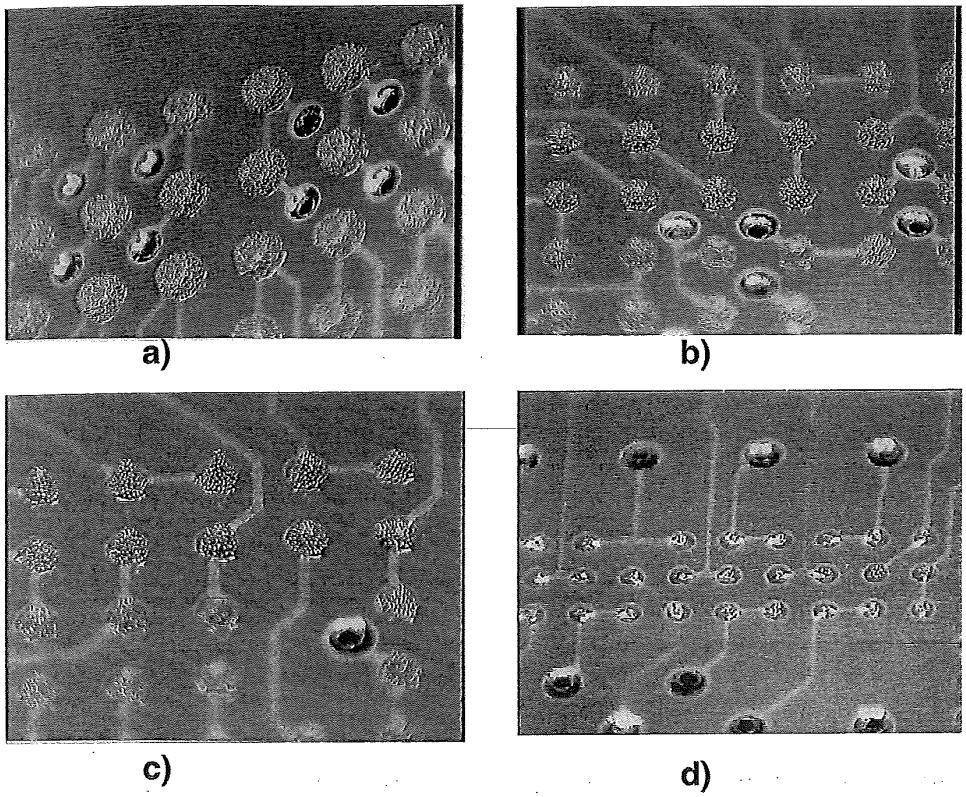


Fig. 18-31 Photographs showing the difference in solder print quality as pitch decreases from (a) 1.0 mm, (b) 0.8 mm, (c) 0.75 mm, to (d) 0.5 mm. All were printed at the time on the same PWB using a 0.006-mil stencil demonstrating one of the problems with a wide variation of component pitches on the same assembly.

for board assembly of CSPs with solder-ball pitches of 0.75 mm. Those CSPs with a finer solder-ball pitch require modifications to the print process. Reducing the stencil thickness to .005″ provides a better release and a more consistent print. However the particle size of Type 3 solder paste minimizes the actual number of solder spheres that fit into an aperture. Type 4 solder paste with finer solder particles provides a higher solids loading in the paste, and thus increases the post reflow solder volume. Type 4 solder pastes are not a dropin replacement for type 3 pastes; that is, new processes, out-life control requirements, and reflow profiles must be re-established. It is important to recognize that as the particle size decreases the total effective surface area and hence the oxide content on the balls increases; this may have some impact on solderability and a more aggressive flux may be required for proper solder-joint formation. The cost of the Type 4 solder paste is also higher than Type 3 [110].

18.6.4 Solder Paste Printing

Solder paste printing is one of the most critical operations in the assembly process as it has a significant effect on assembly yields and reliability. Solder paste bricks should be uniform in shape and volume across the entire CSP pad pattern. Variations in the solder volume can cause bridges, electrical opens, or low volume solder joints that lead to early failure. Also, the lack of a uniform solder

volume makes it difficult to determine the acceptable upper and lower limits for automated solder joint inspection. With area-array components, only one defective solder joint necessitates reworking a component. The effect of the solder paste printing operation on the assembly yields and ultimate assembly reliability is significant [111]. Consistently low defect and predictable reliability result from proper control of print registration, solder volume, and solder paste outlife (exposure in open jar or on screen). What seem to be minor problems with print registration, or variation in paste volume for example, can result in increases in bridging, electrical opens, false or missed calls at x-ray inspection, and lower solder-joint reliability. Paste drying or the loss of volatiles and/or moisture absorption in the solder paste can lead to increased voiding and paste outlife limits should be determined, monitored carefully, and not exceeded. Keeping the stencil clean during printing is essential especially if the time between prints is in excess of 5 minutes or if the unreplenished paste is used for an extended time period. Periodically placing the stencil in a washer is most effective and should be used in conjunction with wiping to prevent clogged apertures.

18.6.4.1 Fine line printing Solder paste printing can be a challenge when dealing with 0.5 mm packages. Stencil thickness, shape and aspect ratio of the opening, surface finish of the board, and the paste characteristics all can play a role in successful printing. It is not uncommon to have print efficiencies of less than 60% on 0.5 mm pitch components. As mentioned above, process modifications for 0.5 mm pitch components can include using square apertures with rounded corners on the stencil, decreasing stencil thickness to .004″, and the use of Type 4 solder paste.

18.6.4.2 Paste vs. flux In some cases CSPs are assembled using flux rather than solder paste. Assemblies using only flux may meet some product requirements but not all, especially the high-reliability applications. The increased height of the solder paste bricks compared to flux paste alone, can help alleviate problems with ball planarity, package planarity, board planarity, and board surface finish flatness. Paste printing also adds solder volume, can increase solder joint height, and improves solder wetting of the pads [112]. Addition of solder paste can play a significant role in assembly yields, as well as reliability.

18.6.5 Solder-Paste Print Inspection

Automated inspection of the solder paste print is recommended for the assembly of the area-array components, particularly CSPs owing to their fine pitch. Missing solder paste on a single pad requires rework since there is no possibility for touch up. To ensure a low-defect assembly operation it is imperative to verify the presence, uniformity, and correct solder-paste volume on the pads. Visual inspection of the paste print can be used but is a slow process, prone to error, and expensive. Automated inspection of the solder paste print can be accomplished using vision, laser, or x-ray systems. The capability is available on many screen printers but they are relatively slow and often provide only 2D inspection. Solder-paste presence, smearing, registration, and bridging can be verified and measured with these systems. However, significant height variation and even conical shaped solder paste depositions may not be identified. These inspection options on the screen printers are improving but do not eliminate a bottle neck on a high-volume assembly line as no additional printing can take place during inspection.

18.6.5.1 Stand-alone systems Automated stand-alone measurement systems can reduce the bottleneck at the printer. Inspections can be performed at the same time the screen printer is printing another board or panel and typically can complete the inspection in less time than it takes for the screen print operation. X-ray inspection is an offline operation that makes volumetric measurement of each solder brick printed. The method is effective but time consuming. It requires operator intervention, removal of

EX. 1004 - Page 64

the boards from the line, and can significantly increase the time between print and the pick and place operation. Inspection of every area array solder pad is recommended even if automated inspection systems are not available.

18.6.6 Component Placement

Component placement and reflow should take place as soon after screen print as possible. Delays allow changes to take place in the solder paste through loss of volatiles or drying of the paste and moisture absorption. These changes may lead to increased voiding in the solder joints under the area array components.

18.6.6.1 Required accuracy for CSPs A benefit CSP components have over flip-chip dice is that they can be placed with existing surface-mount equipment and therefore do not require additional capital expenditures or space on the assembly line. Collapsible solder spheres are commonly used on CSPs and allow greater placement tolerances owing to the self-centering tendencies of the solder sphere [113]. Chip-shooter placement equipment with a placement accuracy of +/−0.05 mm, has demonstrated the capability to pick and place, CSPs (from tape and reel) with solder ball pitches greater than or equal to 0.75 mm at a rate of 4 parts per second. This is a significant improvement over a one part per second rate typical of fine-pitch pick and place equipment [101,114]. The increased rate is mainly due to an allowed misalignment of approximately one half of a pad diameter, which is corrected by self alignment during reflow. Higher precision placement equipment (+/−0.05 mm) operating at a reduced placement rate is recommended for component pitches less than 0.75 mm. The goal, in any event, is to place components as close to true position as possible to avoid the risk of bridging that can occur with poor alignment.

18.6.6.2 Vision systems Pick and place equipment uses several different means of aligning the component to the board; mechanical alignment, black-body vision systems, and array vision systems. Mechanical alignment and vision systems using back lighting or black-body/binary alignment, register on the edge of the package and do not consider the alignment of the solder ball array. Vision systems using array vision combine component alignment of the solder ball array with capabilities for solder ball presence verification. Acceptance of the package using array vision systems is based on the recognition of a minimum percentage of the total number of solder balls on each package, allowing for recognition of damaged or missing solder balls while aligning the solder ball array. Setting the threshold acceptance limit to 100% usually results in a high percentage of false rejects particularly on the high I/O components. Careful adjustment of sensors can minimize rejections but inspection of the BGA to board alignment is strongly recommended prior to reflow.

Manufacturers of pick and place equipment are improving methods for reducing the number of false rejects with improved sensors, algorithms, and lighting schemes and through the use of multiple cameras.

18.6.6.3 Paste contact While placing CSPs the solder balls do not have to make contact with the board. Contact with all the solder paste is sufficient and can be achieved driving the solder balls only 0.05 mm into the solder paste. Coplanarity of the CSP solder balls is typically less than 0.05 mm allowing all the solder balls to make contact using these parameters. Driving the component farther into the solder paste increases the risk of bridging.

18.6.7 Placement Inspection

A placement inspection prior to reflow is the last opportunity to catch assembly problems without having to expose the boards and components to a rework cycle. While operator inspection of correct component presence, alignment, rotation and polarity is

often done for low-volume jobs, high volume operations can take advantage of automated inspection systems now available. These systems can be programmed to identify components by outline and verify part numbers. Components can also be checked for alignment to the pads, polarity, rotation, and orientation. Although these systems require considerable programming and fine tuning, they are effective in pin pointing errors introduced into a run by installation of a new reel or matrix tray with improperly oriented components, as occasionally occurs in high-volume operations. In low-volume high-mix operations where the number of setup changes occurring in a shift can cause confusion, these systems can catch and reduce defects before the boards are reflowed.

18.6.8 Reflow Attachment/Effects

Convection reflow has been shown to be very effective in providing uniform heating of components and PWBs during the reflow process. Measurement of the board and component temperatures in the product form factor is imperative to define effective reflow profiles for manufacturing.

18.6.8.1 Factors that affect profile Heating uniformity is affected by differences in component mass, distribution of components on a board, and PWB differences (e.g., mass, material, stackup, dimensions, etc.), oven type and number of zones, and fixturing. Profiles also vary due to solder paste flux chemistry. The manufacturer's recommended profile should be the initial baseline for each board. Differences in flux chemistry, boiling points, activation temperatures, reflow atmosphere, etc., necessitate matching the thermal response of board and component configurations to a paste manufacturer's processing temperature recommendations. This should minimize defects such as partial reflow, solder balling and voiding. Each of these defects can influence the reliability of the solder joints. Proper solder reflow is not a trivial process and careful attention should be paid to achieving optimum results for each board design.

18.6.8.2 Profile Improper time and/or temperature at the preheat, flux activation, reflow, and cooling steps can create defects in the solder joints. Most components and board materials have been tested and are approved for eutectic Pb/Sn reflow processing. Reflow temperatures should not exceed 220°C without testing to quantify the effects of the higher temperatures on the boards, components, and assembly reliability. Slow cooling rates (<5°C per second) can result in a coarsening of the solder grain structure and increased separation of the Sn and Pb phases.

The melting points of most lead-free alloys are approximately 40°C higher than eutectic Sn-Pb, and with reflow temperatures near 245°C. To minimize the impacts of these higher temperatures it is necessary to use steeper heating and cooling rates to limit the exposure (dwell time) to both boards and components. While this profile modification helps limit the exposure time and temperature, it increases thermal shock, decreases temperature uniformity, and decreases the time to form good solder joints (i.e., bond formation, wetting, joint shape, etc.).

18.6.8.3 Atmosphere Although an air reflow can be utilized, a dry inert atmosphere is recommended during reflow to eliminate oxide growth. If water vapor is present during reflow the tendency for the pad metals and solder to oxidize increases. Utilizing an inert atmosphere minimizes the potential for oxidation during the reflow process, thus enhances solder-joint quality. The inert gas should not exceed 100 ppm oxygen or water vapor and 10 ppm or less for applications requiring high reliability.

18.6.8.4 Effects of moisture The most distinguishing feature of CSPs compared to other IC packages is their smaller size and weight, both a positive and negative attribute. It is positive in the sense that little time is required to heat a CSP component to the reflow temperature; however, if heated too rapidly, cracking and delamination of

EX. 1004 - Page 00

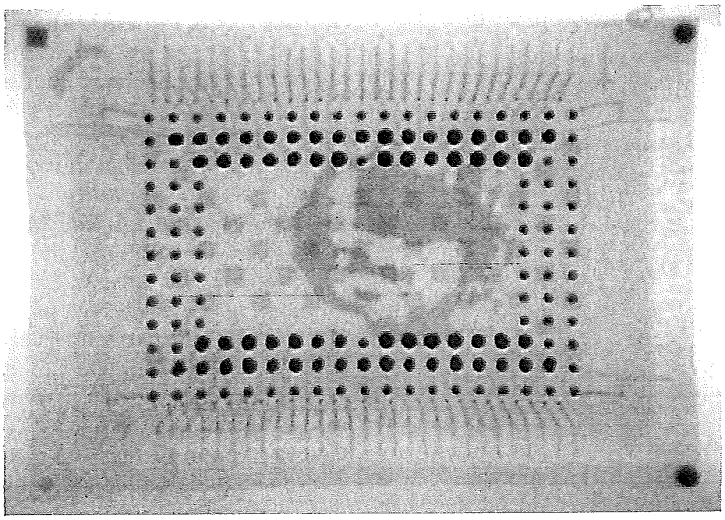


Fig. 18-32 X-ray image of a CSP that was improperly removed with a hot-air type rework system. The dark gray region near the center of the component is solder that wicked into a void caused by moisture induced delamination (popcorning).

the package can occur. The chances of this occurring are increased if absorbed moisture collects along the interfaces of the die and packaging materials. "Popcorning" is the term used to describe packages that have cracked/delaminated due to the rapid vaporization of moisture inside a package during a reflow operation. Cracks and delaminations occur with an insufficient opportunity to dissipate the pressure build up. Internal damage can occur which is not detectable by visual inspection, and which degrades the package performance or reliability. Thin, molded packages (e.g., Thin Small Outline Packages or TSOPs) are the most prone to this kind of damage, but many of the CSP designs utilize a similar structure. Popcorn-type failure of a CSP is depicted in Fig. 18-32. The CSP, part of a popular digital camcorder assembly, was mounted on a small interposer card and underfilled, then the sub-assembly was soldered to the main board to promote reliability by eliminating the need to underfill the component if attached directly to the main board. However, the assembly was not baked out prior to being heated to reflow temperatures, resulting in delamination between the bottom side of the CSP, which is a polyimide film, and the underfill. Solder wicked in and shorted several interconnects together in a void created by the delamination. This shorting was only observable by X-ray inspection.

18.6.9 Cleaning

No-clean, or low residue fluxes are extensively used in card-assembly operations owing to their obvious cost advantages. This is a trend that is expected to increase for assemblies using CSP components and as pitches decrease because of the difficulty of getting cleaning fluid into the small gap between a component and board. However many assembly houses still clean flux residues with aqueous or semi-aqueous solvents to improve solder wetting characteristics (i.e., yields) and bonding of underfill materials, or to meet contractual requirements that demand no visible residues even if they are benign.

Most CSPs can be cleaned adequately with conventional in-line cleaning systems. It is advisable to work closely with both the solder paste and cleaning equipment vendors.

Cleaning fluid entrapment beneath CSPs is common. It is important to remove entrapped fluids prior to packaging and especially if the assemblies are to be conformally coated.

18.6.10 Assembly Inspection

Cost and cycle time reduction drive efforts to eliminate inspections, however some inspection is usually required to monitor the assembly process to ensure that it is in control. Inspections can be of a limited nature on a small sample of low-cost boards to 100% for high-value or high-reliability applications. Visual, x-ray, and acoustic microscopy are the three common post-assembly inspection techniques. Automation is reducing the cycle-time requirements for each of these techniques. Although no technique guarantees a defect-free assembly, each can be used to identify an out-of-control process and minimize defects that escape to the field.

18.6.10.1 Visual inspection Visual inspection can be used to evaluate a small quantity or samples of assemblies but is extremely costly in terms of labor, cycle time and escaped defects. Although inspection of leaded components is reasonably effective, only perimeter solder joints are visible on area-array CSPs. Often evaluations are limited to partial views of the solder joints since the line of sight is obstructed by neighboring components and low stand-off height of CSPs. Visual inspection can be useful in identifying process related problems such as skewed solder joints or partially reflowed solder joints. Line-of-sight and low stand-off height limitation also restrict automated visual inspections of CSPs to component presence, registration, and orientation.

18.6.10.2 X-ray inspection X-ray inspection equipment offers the capability to inspect the interior solder joints on CSPs and is a valuable tool for process development and production solder joint inspection. There are two types of systems available, transmission and laminography. An important aspect of x-ray examination is its sensitivity to high density boards and different core materials embedded in the printed wiring board for CTE constraint. Cores comprised of large atomic weight elements such as molybdenum, copper-invar-copper and the like absorb x-rays and render the technique less effective. X-ray inspection can effectively detect missing balls, solder bridges, grossly inadequate solder joints and solder voids (Fig. 18-32, white areas). Examination for voids should be carried out judiciously since power and frequency settings can either exaggerate or underestimate the voiding effects [32,33]. Also, marginally good solder joints can be difficult to discern by x-ray techniques. Cracks or poor wetting of a pad on a board can remain hidden due to the limitations of these systems.

18.6.10.3 Acoustic microscopy An inspection technique using ultrasonic energy at the component level is termed acoustic microscopy owing to the capability to detect extremely small defects and is another tool used to detect defects in circuit board assemblies. This technique requires a coupling agent, usually water, to provide a continuous path for sound wave propagation. It can be effective in identifying the location of any discontinuities such as cracks, delaminations, and voids, in components, underfill materials, solder joints and boards. Ultrasonic energy must be introduced perpendicular to the surface of inspection making inspection of curved surfaces difficult. For CSP assemblies, the technique is currently best suited for inspection of selected components with similar construction and not every component on the board. Variation in the acoustic signal response from dissimilar components may require numerous programs and/or frequency changes to optimize the inspection results. The technique is very effective for low volume or development operations, and failure analysis applications.

18.6.10.4 Voids Voids can be defined as bubbles or cavities within a solder joint. Chip scale packages can sometimes have voids in the as-received solder balls, depending on the

EX. 1004 - Page 68

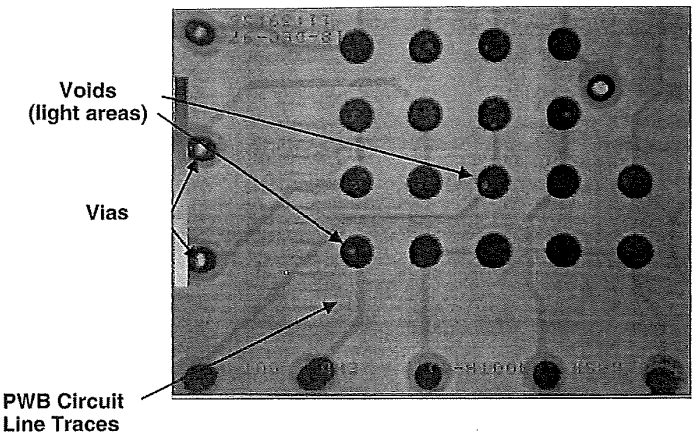


Fig. 18-33 Through transmission x-ray showing PWB features along with voided CSP solder joints.

ball-attachment technique. The reflow operation can also cause voids during assembly [115]. Several hypotheses have been proposed for their formation: volatile species, produced as a result of the thermal decomposition of flux constituents, or oxide films that get entrapped in the solder matrix, etc. [116,117]. Reduction of metal oxides by flux can generate species such as hydrogen, carbon dioxide, water vapor, etc., depending on the nature of the flux. Volatile constituents such as solvents in the flux paste, additives for thixotropic modification, water vapor entrapped in the paste, and moisture exuded from the laminate are also cited as sources for voiding.

The reflow process parameters that influence void formation are: ramp-up rates, flux activation temperature and activation dwell time, maximum reflow temperature, dwell time above reflow temperature, and ramp-down rates. Ramp rates of 2–4°C/s are suggested to avoid paste splashing. A linear correlation between oxygen content in the 100 to 1200 ppm range in a reflow oven and the extent of voiding has been observed. Surface porosity also favors void formation as does metal content and decreased particle size because both tend to increase oxide content which in turn affects voiding. Elapsed time between paste printing and reflow can also have an effect on voiding. If the soak time is not optimized, it may limit the expulsion time of volatilized material leading to entrapment [118]. Soak times of the order of 2.5 minutes or slightly longer, and low peak temperatures in the vicinity of 205°C seem to minimize voiding. Figure 18-33 shows voids as seen under CSPs using through-transmission x-ray, and Fig. 18-34 using x-ray laminography.

18.7 CSP Rework

Controlling individual process steps reduces the additional cost and cycle time incurred by rework. It has been shown that reworked solder joints without the addition of solder paste can meet and exceed the

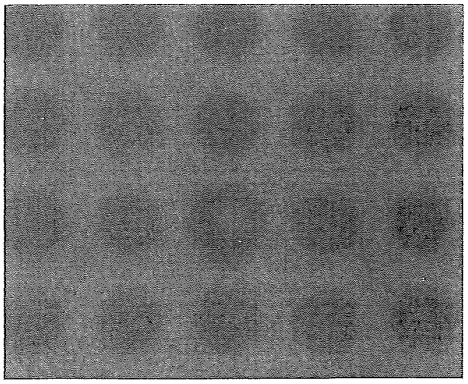


Fig. 18-34 Void shown in x-ray laminography image.

Table 18-8 Partial list of rework equipment manufacturers

Company	Location	Phone
Air-Vac Engineering	Seymour, CT	203-888-9900
Advanced Techniques Co.	Pennsylvania	215-364-5588
APE Corp	Key Largo, FL	305-451-4722
Austin American Technologies	Austin, TX	512-335-6400
Conceptronics	Portsmouth, NH	603-431-6262
Fine Tech (Palomar Products)	Carlsbad, CA	619-931-3622
Manix	Huntingdon Valley, PA	215-953-9797
MRSI	Chelmsford, MA	508-256-4950
OK Industries	Yonkers, NY	914-969-6800
Pace	Laurel, MD	301-490-9860
PDR Microelectronics	Pleasanton, CA	510-455-8602
SEC	Moorpark CA	805-529-2293
SRT	Westford, MA	508-392-0633
Wenesco	Chicago, IL	312-973-4430

requirements for extended-temperature-range applications, but the reduced solder volume is likely to reduce the reliability compared to non-reworked solder joints [112]. However, where possible, additional solder paste should be added when replacing an area-array package [119]. Micro stencils are commonly used for this purpose but can be difficult due to limited space. It is also difficult to hold a stencil steady, cover all the openings in one sweep, and remove a micro stencil cleanly. The practice and skill required to master the art of micro stencil printing should not be underestimated.

18.7.1 Rework Equipment/Tooling

Although there are a number of companies that manufacture equipment to rework defective assemblies, only a few machines are capable of reworking BGA components; and even fewer for CSPs, which in most cases are miniature, fine-pitched (e.g., 0.5 mm) area array packages. A partial list of companies offering equipment and/or tools for CSP rework is given in Table 18-8. Based on a review of the literature and industry practice, the basic equipment features considered necessary for reworking CSPs on a large-volume basis are noted in Table 18-9. Most commercial systems utilize hot gas directed and contained by nozzles designed for specific component sizes and shapes. A vacuum tool inside the nozzle holds a replacement component over the rework site (see Chapter 20). The CSP self aligns when the solder balls become molten.

18.7.2 Thermal Profile Monitors

A thermal profile must be established that can be utilized for both removing a CSP and attaching the replacement component. Initially, a multi-purpose test vehicle can be utilized such as the one shown in Fig. 18-35. This vehicle includes two component sites for 12.7 mm square, 188-pin daisy chain Tessera's μBGA®; along with four wire-bonded sites and four flip-chip sites. The test vehicle shown in the figure is 18-mils thick, contains 6 metal layers, and is the size of a PCMCIA[1] card, with a gold flash (0.1 μm thick) on a nickel overplate. The hidden nature of CSP solder joints requires careful thermal profiling to assure that all solder joints are completely reflowed. In addition to profiling at CSP sites, thermal measurements of the board and adjacent components helps insure the rework process does not functionally degrade other portions of the assembly. As a final check, a test vehicle should be constructed utilizing a product card/board or one whose form factor closely resembles the product for verification purposes.

[1]Personal Computer Memory Card Industry Association

EX. 1004 - Page 70

Table 18-9 Basic features recommended for CSP rework equipment

Split-beam imaging system	Allows the operator to see a magnified image of the bottom side of a CSP superimposed over the corresponding land pattern on the PWB during alignment before placement (see chapter 20).
Separate light sources	Used for viewing board and component, each independently controllable by the operator.
Localized topside heating	Either forced convection (flowing hot gas) or by radiation (focused infrared beam) that is sufficiently localized to avoid adversely affecting nearby components.
Auxiliary underside heating and support	Helps minimize board warpage that can occur due to the intense localized topside heating. Using an auxiliary heating system to preheat the board also minimizes the time and temperature required for localized heating of the top-side components.
Universal tooling	Tooling must not be too sensitive to CSP configurations; i.e., the capability of utilizing the same tool for a variety of shapes and sizes.
Positioning control	Coarse and fine positioning of the assembly repaired.
Software	Configured for rapid set-up, thermal profiling, and process control.
Component size	Capability of handling components up to 1 inch square.
Assembly size	Capability of handling assembly sizes up to 300 mm × 400 mm (12″ × 16″).

18.7.2.1 Thermocouple placement For most area array packages such as plastic BGAs, tape BGAs, and ceramic BGAs, fine-gauge thermocouples are bonded directly onto several pads prior to placing a component. This technique provides highly reliable information on solder-joint temperatures. However, any attempt at installing thermocouples to the extremely small pads of CSP components would likely destroy them. As a result, thermal profiling of CSPs is typically limited to monitoring the package rather than joint temperature. The small size and low thermal mass of CSPs make this an acceptable profiling approach. The test vehicle is configured with the thermocouples (5-mil gauge type K) installed on top of the CSPs and the topside of the substrate/chip carrier (125-mils away). Adjacent CSPs are typically located 100-mils away.

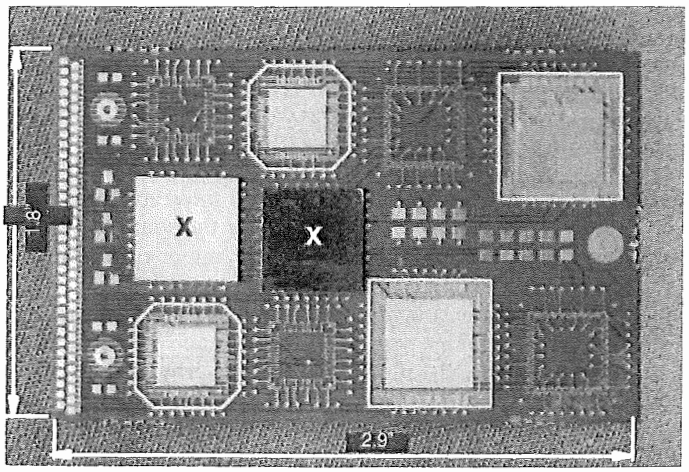


Fig. 18-35 Photograph of a rework test vehicle containing various types of components. Xs indicate μBGA sites.

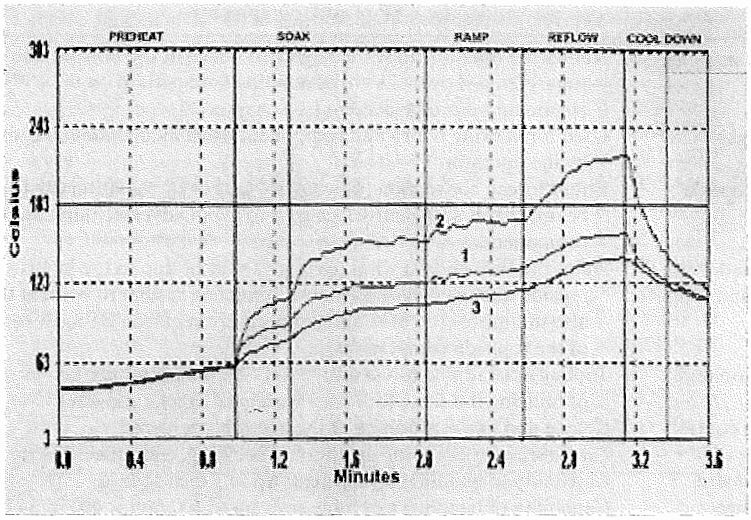


Fig. 18-36 Typical thermal profile used for the 12.7 mm (0.5″) square μBGA component. Thermocouple measurements were taken 1) on the PWB at a distance of 0.125″ from the CSP, 2) on top of the CSP, 3) on an adjacent component.

18.7.2.2 Thermal profile A typical thermal profile (Fig. 18-36) usually includes the preheat, soak, ramp, reflow and cool-down stages. In the figure the package temperature achieved a maximum of 223°C and the period above 183°C (dwell time) is approximately 40 seconds. The average slope during the heating cycle is about 1°C per second. Also, the temperature of adjacent devices and substrate/chip carrier in close proximity to a reworked CSP site (not shown in the figure) is to be sufficiently low so as to minimize adverse effects on functionality and reliability, and avoid partially melting any solder interconnections.

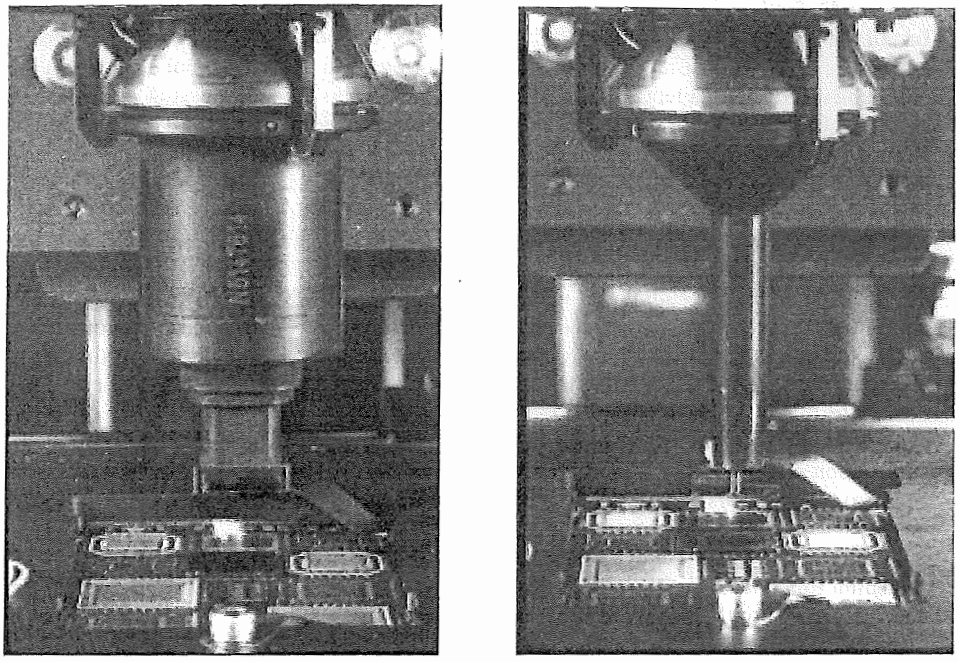
18.7.3 General Rework Process Flow

A typical surface-mount-component rework process consists of removal of a defective component, site dressing or preparation, addition of flux paste or solder paste, placement of a new package and reflow. In the case of CSP solder joints, where hand touch up of the solder joints is not feasible, rework implies replacement similar to BGA replacement. Since CSP components are much smaller in size than their BGA counterparts, improved tools or a modified procedure may be required. Placement accuracy is more critical but the removal and reflow of CSP components is often easier than with BGAs due to their low thermal mass. BGA rework design, process, and equipment information may be found in references 120–123, and is covered in detail in chapter 20.

Once an acceptable thermal profile is established, the process for reworking CSPs that have not been underfilled proceeds as follows:

- Dryness of Assembly
  Dry the assembly for 24 hours at 125°C prior to any reflow soldering operation to remove moisture from all plastic components on the board and prevent popcorning of the components or delamination of the board.
- Avoid Flexure
  The assembly is placed in the rework system in a way that it will not flex when moderate placement pressure is applied or during exposure to a reflow cycle. When assemblies are very thin, a pallet cut out constructed of a heat-resistant material like Delmat™ should be used.

- Remove Defective CSP
  Install the assembly in the rework machine and preheat the board, apply tacky flux paste and remove the defective device with a pre-established thermal profile.
- Remove Residual Solder
  Apply additional tacky flux paste to the site as required, lower the nozzle (without a component loaded), and reflow the site. When the pads are fully reflowed, the nozzle is lifted and a vacuum tool with a Teflon® tip is used to remove excess solder. A solder wick or other solder-removal technique may be used for this step, but non-uniform pad height is often the result. Care must be taken not to damage the small pads or solder mask. Nozzles are available from several vendors that apply localized heat to reflow the solder on the pads and at the same time remove the excess through a vacuum tube located at the center of the nozzle. A fixed nozzle height produces uniform solder volume on the pads and minimizes the risk of lifted pads and/or damage to the solder mask.
- Clean Flux
  Remove residual flux with isopropyl alcohol and a lint-free swab or wipe. Vacuum removal of the alcohol and flux mixture can minimize spreading of the flux under adjacent components and thereby simplify cleaning.
- Assure Planarity
  Inspect the site for pad uniformity. If the pads appear to be non-uniform in height, repeat the site-dressing process. It is very important that the pads be uniform to avoid coplanarity issues during the replacement process.
- Avoid Contact
  When replacing a component, great care should be taken not to touch the ball side of the device with bare hands as skin oils may interfere with solder wetting. Vacuum pencils and/or gloves should be used to handle the components.
- Align Replacement CSP
  The component is aligned using a split-beam imaging system that allows the operator to view an image of the component bottom (i.e., solder balls) which is superimposed on the corresponding board pads. The beam splitter not only aids in assuring good alignment, but also allows the operator to see any missing or deformed solder spheres on the CSP and missing or damaged pads on the board.
- Apply Flux
  Once the component is aligned, tacky no-clean flux is applied to the site. It is important to use a "tacky" formulation or flux paste rather than a liquid formulation because liquid fluxes evaporate too quickly. This step must follow the alignment step since applying flux prior to alignment causes viewing problems in the beam splitter. Due to the small size of CSP components, care must be taken not to apply too much flux.
  (a) Brush
  A fine-tipped artist's brush is adequate for applying a suitable amount of flux.
  (b) Dipping
  Excellent results have also been achieved by "dipping" the component into a known thickness of flux paste. A batter bar or squeegee is used to produce a uniform thickness of paste. The paste height should be approximately one half the height of the solder balls on the package. This step takes place before alignment of the pads and component [124].
  (c) Micro Stencils
  Micro stencils can also be used to print solder paste onto the pads. However this requires a great deal of skill to be successful. For those skilled in the art, solder paste offers an increase in solder volume and is reported to improve the wetting and formation of solder joints [112].
- Placement
  A replacement component is placed using the same nozzle used for component removal. Two different nozzle types, similar to those shown in Fig. 18-37, may be used for CSP placement. It is best to apply some force when placing CSP components to help overcome coplanarity differences. However, force should eliminated prior to



(a) (b)

Fig. 18-37 Two placement nozzle designs used in placing CSP components. (a) is specially designed for 12.7 mm (0.5″ μBGAs, (b) is designed for a range or μBGA and flip chip devices.

reaching reflow temperature to avoid component collapse, and allow a component to self center and assume a height determined by the molten solder surface tension.

- Replacement CSP Reflow
  Since the solder connections of CSPs are typically beneath the component in an array format, the solder joints are reflowed by heating through the package rather than by direct heating as is typical for peripherally-leaded components. Some equipment manufacturers claim there is an advantage to using heated air directed beneath a component to help assure that the entire component achieves requisite reflow temperature. Directing air underneath lightweight CSPs can cause a component to shift leading to skewed solder joints, bridging, or transfer of the solder paste from one solder joint to another leaving some joints with insufficient solder or an open. Direct heating through the CSPs can also produce consistent results.

A total rework time of approximately 20 minutes per CSP is not unusual. This includes loading the assembly, removal of the component, site dressing/cleaning, alignment, placement and reflow. Profiles for removal and for replacement may be different.

18.8 Reliability of CSP Assemblies

Although CSPs provide significant space, weight, handling and performance advantages for numerous applications, their reliability at either the component or board level is typically a concern to many engineers. Tables 18-10 through 18-12 include many CSP-related reliability tests and results cited in references [4,5,31,43,58,125–138]. The tables indicate individual semiconductor manufacturers have their own test methods and test conditions depending upon their customers' needs and applications. These data may not be directly applicable to every CSP

application, but can serve as useful references. Also, it is important to recognize that CSPs of the same type from different suppliers may have different material sets in their construction.

18.8.1 Packaging Levels

Reliability of the chip-scale assemblies needs to be addressed from several viewpoints. First there is package reliability, then there is board-level assembly reliability, and finally there is the box or system-level reliability. While a package may successfully pass a battery of reliability tests, it may experience fails when tested at the board level because the interaction between board and package characteristics may induce additional stresses leading to product failures. Additionally, when a printed wiring board is incorporated into a box, depending on the manner in which it is assembled and the stresses it is subjected to, it may experience stress distributions different from standard tests and hence different failure mechanisms. It is imperative to assess component reliability at all levels of packaging.

Conventional reliability tests include thermal cycling, thermal shock, pressure cooker tests, temperature-humidity-bias, high-temperature storage, etc., at the package level. At the assembly-level, testing typically consists of thermal cycling, ship-shock, drop-test insulation resistance test, torque, and vibration. At the box-level testing may include thermal cycling, thermal shock, vibration and drop tests. The levels at which these tests are performed generally depend on product and its life requirements.

18.8.2 Chip Carrier Effects

For example, the substrate for a CSP may be rigid glass-reinforced bismaleimide triazine laminate, polyimide tape, or alumina type ceramic substrate with a wire bonded die. Another construction may consist of a polyimide tape with an elastomeric material between the die and polyimide tape. The TAB-type beam leads are bonded to the die similar to a microBGA®. The construction of CSPs has a significant influence on board-level reliability. For example, it was shown that a change in the base material for a CSP from polyimide to BT resulted in higher reliability in a similar test [139]. This was attributed to the thicker BT resin substrate which provided a better CTE isolation of the die from the solder joint. A similar CTE isolation is provided by a silicone elastomer layer in microBGA®-type packages. In the case of CSPs with TAB-type ribbon bonds, package failures have been found at the heel or in the middle of a ribbon.

18.8.3 Board Effects

18.8.3.1 Thickness Board thickness can play a significant role in the reliability of CSP solder joints. Decreasing the board thickness from 62-mils to 16-mils has shown as much as 2X improvement in board level reliability [140].

18.8.3.2 Single versus double-sided assembly Chip scale package reliability can depend on the manner of board population. The fatigue life of double-sided assemblies subjected to a condition A test (−30 to 100°C) with mirrored packages is about half that of single-sided assemblies. However, staggering the packages on double-sided assemblies improved fatigue life [141].

18.8.3.3 CTE mismatch Circuit card assemblies with extreme CTE mismatch between the component and the board can experience solder joint failures in as few as 40 cycles in 0 to 100°C thermal cycling, while CTE matched assemblies (e.g., ΔCTE <5 ppm) survive in excess of 1000 cycles even in −55 to 125°C [142].

Other factors such as via misregistration or solder mask coverage on the pads can aggravate a CTE mismatch problem while increasing solder ball diameter or underfilling can improve the problem. For example, larger solder balls generally enhance solder joint

Table 18-10 Published reliability test data reported by various CSP suppliers

Supplier	Package	Test	Test Conditions	Failure #/N
Intel	4 Mb flash structure = μBGA	Temp. cycle B (FR4 interposer)	−55 to +125°C, 1000 cycles	0/78
	I/O = 46	Temp. cycle C (ceramic interp.)	−65 to +125°C, 1000 cycles	2/78 (4 WBs failed)
	Pitch = 0.7 mm	THB (ceramic interp.)	85°C/85% RH, 1000 hrs	0/78
	Size = 3.75 mm × 5.25 mm approx.	HAST (ceramic interp.)	130°C/85% RH, 150 hrs	0/28
		Level 1 precond. (pkg)	85°C/85% RH, 168 hrs	No delamination or crack
		High temp. storage (pkg)	150°C, 1000 hrs	0/78
Fujitsu	16 Mb DRAM structure = SON	Temp. cycle test	−65 to +150°C, 1 hr/cycle, >500 cycles	0/40
	I/O = 26	Package crack (pkg)	85°C/85% RH, 168 hrs, heat up to 245°C	0/100
	Pitch = 1.0 mm Size = 7 × 16 mm	Temp. cycle test (pkg)	−65 to + 150°C, 500 cycles	0/25
		PCT (pkg)	121°C, 2 atm. press, 100%, 336 hrs (pre-cond.: 85°C/85%, 168 hrs + IR)	0/25
Hitachi	DRAM structure = TAB tape-based CSP	Temp. cycle test	−55 to +125°.C, 1500 cycles	0/21
	I/O = 40	High temp. and humidity (pkg)	85°C/85% RH, 408 hrs	0/19
	Pitch = 1.0 mm	PCT (pkg)	121°C, 2 atm. press, 480 hrs	0/41
	Size = 11.5 mm × 6.6 mm	High temp. storage (pkg)	150°C, 1000 hrs	0/11

EX. 1004 - Page 76

Table 18-10 (*Continued*)

Supplier	Package	Test	Test Conditions	Failure #/N
LG Semicon	Test chip structure = BLP I/O = 20 or 28	Temp. cycle test Preprocessing (pkg)	−55 to +125◦C, >800 cycles 85°C/85% RH, 168 hrs	0/6 No delamination or crack
	Pitch = 0.5 mm Size = 11.72 mm × 5.21 mm	Thermal shock (pkg)	IR reflow @ 240°C, 3X	No delamination or crack
Mitsubishi	Test chip structure = MCSP I/O = 96 (6 × 16) Pitch = 0.8 mm Size = 6.35 × 15.24 × 0.65 mm	Temp. cycle test (96 MCSP)	−40 to +125°C, 1 hr/cycle, 200 cycles −40 to +125°C, 500 cycles	0/20 8/20
		High temp. and humidity (pkg) (1024 MCSP)	85°C/85% RH, 48 hrs, heat to 235°C max.	No delamination or crack (0/5)
Sharp	Test chip I/O = 160 Pitch = 0.8 mm Size = 12 × 12 mm	Temp. cycle test High temp. and humidity Repeated bending test (Bd Size = 100 × 50 × 0.6 mm)	−40 to +125°C, 300 cycles 85°C/85% RH, + 7.0 V, 1000 hrs The mounted position is fulcrum. Bend 2 pts. on bd. w/2 mm deformation. 300 cycles.	0/18 0/25 0/10
	Structure = PI/Cu	Package crack (pkg)	30°C, 75% RH, 96 hrs; heat to 230°C, 2 cycles; PCT (121°C, 1 atm., 100% RH), 300 hrs	0/32

Table 18-11 Mini BGA solder ball shear data reported by various CSP suppliers

Test	Specification	Sample Size	Results	Comments
Ball shear	—	4 wafers	Avg. = 206 g	PI dielectric
Ball shear	—	1 wafers	Avg. = 197 g	BCB dielectric
Thermal cycle (FR4 board level)	Air to air, 0 to 100 degree C	12 dies	10 to 40 cycles	No underfill
Thermal cycle (FR4 board level)	Air to air, 0 to 100 degree C	12 dies	>2000 cycles	With underfill
Thermal cycle (FR4 board level)	Air to air, −55 to 125 degree C	8 dies	>500 cycles	With underfill

reliability through an increase of solder volume and an increase in height. It has been shown that the stress on the solder joint is inversely proportional to the height of the solder joint or in other words, less stress is induced in taller solder joints.

18.8.4 Surface Finish Effects

18.8.4.1 Standard finishes Surface finishes of the printed wiring board and laminate chip carrier can have a significant impact on board-level reliability. The laminate surface finish is organic solder preservative (OSP) such as benzotriazole, imidazoles, or polyalkyl benzimidazoles, nickel, immersion gold over nickel, or in other cases the tin/lead is plated over the barrier metal and reflowed to form the ball. The barrier metallization is typically Ti/Cu, Al/Ni/V/Cu, Ti/Ni or Ni. Common PWB surface finishes are immersion gold over nickel, hot air solder level (HASL), OSP, white tin, or plated and reflowed Sn/Pb. The finish required for assembling fine-pitch CSPs with an acceptable yield requires a flat or planar surface.

18.8.4.2 Metallurgical factors OSP and immersion gold over nickel are preferred for fine-pitch CSP assemblies owing to the planarity offered by these finishes, but they differ in the nature of the solder joints formed. With both HASL and OSP, Cu-Sn intermetallic constitutes the metallurgical bond between the surfaces. In the case of Au over Ni, Ni-Sn intermetallic constitutes the metallurgical bond. The gold helps preserve the solderability of the surface and dissolves into the bulk of the solder some of which precipitates as dispersed Au-Sn intermetallics which slightly strengthens the joint.

Gold thickness effects. Excessive gold content (>3% wt) is deleterious, embrittling the joint. Thus, Au thickness must be minimized for CSP applications. On the other hand, very thin gold deposits can be porous leading to the oxidation of the underlying nickel thus producing a surface which is

Table 18-12 Mini BGA accelerated thermal cycling reliability tests

Test	Specification	Die Pad	Substrate Pad	Test Results
Thermal cycle (on Si substrate)	Air to air, 0 to 100 degree C	Au	Adhesive and au	>1000 cycles
Thermal cycle (on Si substrate)	Air to air, 0 to 100 degree C	63Sn/37Pb	63Sn/37Pb	>1000 cycles
Thermal cycle (on Si substrate)	Air to air, 0 to 100 degree C	63Sn/37Pb	63Sn/37Pb	>1000 cycles
Thermal cycle (on Al_2O_3 substrate)	Air to air, 0 to 100 degree C	63Sn/37Pb	5Sn/95Pb	>1000 cycles

difficult to solder to. Migrating from 1.27-mm pitch to 0.8, 0.76, and 0.5-mm pitch CSP assemblies, the gold intermetallic problem may become even more severe. The solder volume is much smaller in these joints in comparison to a joint in 1.27-mm pitch package, while gold thickness remains the same on both the pads. Thus the effective weight percent of gold in a CSP joint will be higher than in the 1.27-mm pitch joint. It is important to be cognizant of this fact. A 0.8 to 1.27 micron Au layer has been recommended for microBGA® and CSP pads. A decreased Au thickness will increase the potential for porosity in the film which increases the chance of forming a non-wettable NiO layer on the pads. An OSP surface may yield a higher product life compared to a Ni-Au surface on the PWB [143].

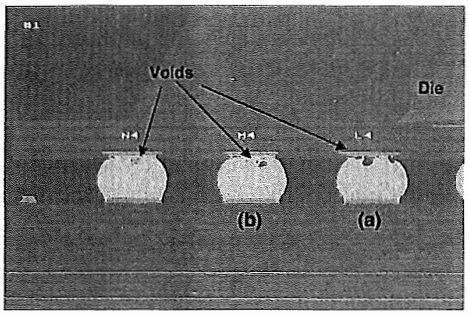


Fig. 18-38 Metallographic cross section of a row of organic carrier CSP solder joints, some of which contain voids. The position of voids in a solder joint, the size, and the location of the voided joint in relation to the edge of the die (with organic carrier, DNP for ceramic) are important from a reliability perspective. The significance of voids decreases as the distance.

Black pad. In addition to oxidation, the wettability of a pad surface is also influenced by the phosphorous content in the nickel [144]. Sporadic solder joint failures by mechanical means have been reported in the literature [145]. A so-called "black pad condition" that affects the wettability of a nickel surface was identified [146,147,148]. Advanced corrosion of a nickel surface by the gold plating chemistry, induced by a charge imbalance between PWB and the ionic species within in the Au plating bath was reported [149]. The consequence of the black pad is partial to total nonwetting of an overplated nickel pad. This may result in poor ball attachment strength and hence either time-zero fails or reduced reliability during testing or in the field.

18.8.5 *Effects of Solder Joint Voids*

18.8.5.1 A problem or not The effect of voids on solder-joint reliability has been a subject of considerable discussion and investigation in the literature. Opinions range from voids being stress arrestors to constituting a very high risk of failure. Large voids can affect not only the mechanical robustness of the solder joints and their thermal properties, but also influence the transmission of high frequency signals and reliability in general [150]. In one study it was indicated that voided areas up to 20% of pad area did not have any negative effect on plastic ball grid array board level reliability. Solder joints with voids, it was indicated, showed 16% better reliability [151]. Whether voids create serious problems depends on the number, size and location of the voids. For example, Fig. 18-38 shows a condition in which voids impact reliability and another where the impact is insignificant due to the location of the void.

18.8.5.2 Influences A joint with an enclosed void will have a higher volume compared to one without voids. The increase in volume may be manifested as a slightly taller joint. With an increased height one would anticipate better reliability. The inclusion of voids in a joint reduces its uniformity and cross sectional area thus reducing the physical properties of the joint. The distribution and location of voids is also a factor. Consider for example situations where a number of voids are lined up along a crack propagation path or a large void is located at the joint-pad interface effectively reducing the bond-pad area.

The number, size, and location and the disposition of the voids is usually not

predictable. Thus it is prudent to minimize the occurrence of voids by the appropriate choice of the paste and by process optimization. Voids in chip scale package assemblies can be a greater reliability risk compared to other area-array packages owing to their smaller joint size.

18.8.5.3 Standards There are no current standards for acceptable levels of voids in area-array assemblies. A proposed acceptance standard for all area-array packages is that voids in the joint shall not exceed 20% of the ball diameter. In addition no single void should be at the exterior of the joint. Multiple voids may be present in a joint as long as the sum total of the voids does not exceed the 20% of the solder joint diameter [152].

18.8.6 Underfill Considerations

For application in harsh thermal mechanical shock and vibration environments, chip scale package assemblies may require reliability enhancements through underfilling. Underfilling CSP assemblies is very similar to flip-chips attached to organic laminates. Similar considerations apply. The integrity of adhesion of the underfill material to the solder joint, the package substrate, and the board soldermask are important. Also, the uniform distribution of the filler material within the underfill matrix is important. Settling of the filler may lead to an even greater CTE mismatch at the interfaces than without an underfill.

Adhesion of underfill materials to the PWB, component and solder joint is critical to the ability of the underfill to enhance reliability. The pressure cooker test is a convenient test to discover or force electronic assembly failures in a short period of time to eliminate weak links potentially detrimental to assembly reliability. Interfacial degradation, swelling, delamination, and corrosion can be detected and understood without regard to acceleration factors that correlate to field performance. Huang et al. have recently reported the effects of underfill on the pressure cooker test performance of Flip Chip on Board Assembly [153]. Figure 18-39 shows a solder-joint crack, underfill/passivation layer delamination, and underfill/solder delamination, indicating an interfacial adhesion weakness. The presence of flux residues, contamination, and the nature of underfill materials can all contribute to such defects. The figure depicts an example of filler settling in the underfill, along with cohesive failures at each interface and solder-mask delamination on the board side. Epoxy under high-humidity conditions, and the accompanying stresses on the constrained underfill results in interfacial failures.

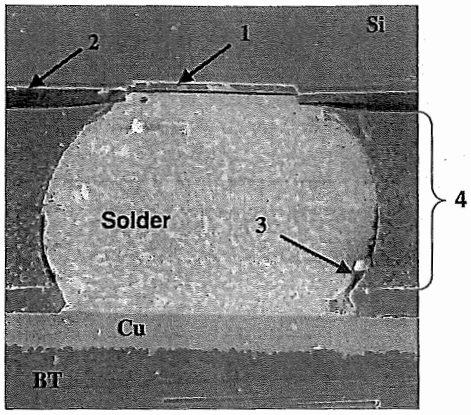


Fig. 18-39 Metallographic cross section of a CSP solder joint surrounded by underfill after subjection to a pressure cooker test. Affected features include (1) separated solder joint, 2) delamination at the underfill/die passivation interface, and 3) delamination at the underfill/solder interface. Settling of the filler material in the underfill can also be seen 4). (Courtesy of Yu-Wen Huang).

18.8.7 Reliability Test Results

Puligandla et al. investigated the board level reliability of 40, 32, and 30 mil pitch packages [91]. Failure data were analyzed and fitted to a standard two-parameter Weibull distribution shown in Fig. 18-40. The first failures occurred at 1163, 1687, and 266 cycles for the 156 I/O 40-mil pitch BGA, 144 I/O 32-mil pitch BGA and 46 I/O 30-mil pitch packages, respectively. The Weibull plots of the three types of packages indicate different slopes

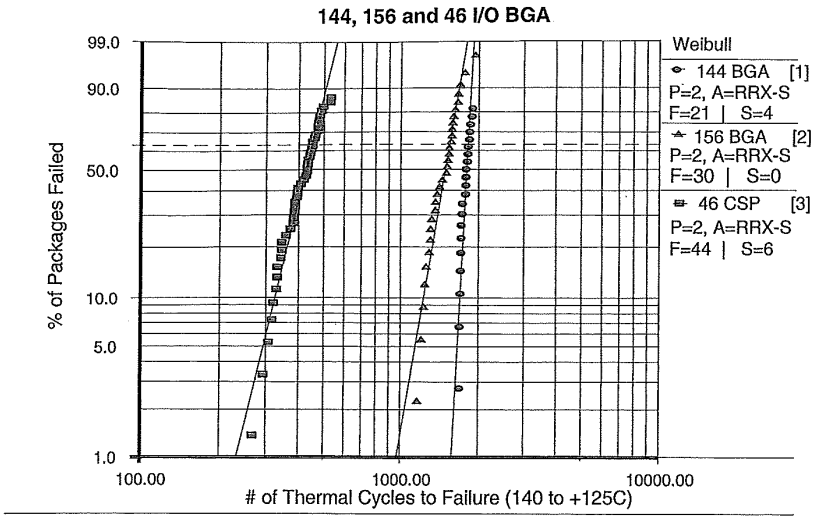


Fig. 18-40 Weibull plot showing the relative reliabilities of three CSPs after thermal cycling on the same test board. Failures for the 144 and 156 I/O components were solder joint failures while the 46 I/O components had internal ribbon bond failures.

with the 144 I/O package showing the steepest slope with a beta value of 31.9. This indicates that most of the packages failed within a small range of cycles. It is not uncommon for fine-pitch area array assemblies to exhibit such large beta values [17]. Two types of failures were observed for both the 156 and 144 I/O packages: solder joint failures and laminate failures described in the following sections.

18.8.7.1 Expansion mismatch effects Solder-joint failures on the 156 I/O package assemblies were observed predominantly on the package side. The ball mounting pads on this package are solder mask-defined. The location of the failures is in the vicinity of the edge of the silicon, a region where there is an abrupt change in the coefficient of expansion (CTE) (Fig. 18-38). The severity of the joint crack decreases the farther away the joints are from this region as can be seen from extremity joint marked N4 in the same figure.

18.8.7.2 Laminate failures Another type of failure that is observed on this assembly is laminate failures in the area adjacent to the solder-mask defined pads on the package side as shown in Fig. 18-41. Board-side cracks on either side of the pad are also observed on the non-soldermask defined pads. The location of crack initiation is at the solder-mask termination on the laminate. In some cases the crack propagates within the laminate structure and along the glass epoxy interface (Fig. 18-42).

Typical failures on the 144 I/O package were similar to those found on the 156 I/O package. Solder fatigue cracks were most likely to occur on the package side of the board near the perimeter of the die as shown in Fig. 18-38.

18.8.7.3 Effect of key factors Neuman and Yuan reported a preliminary evaluation of eight different daisy chained chip scale packages in the 0.8 to 0.5-mm pitch range and 40 to 256 I/O for board level thermal cycling reliability in 0 to 100°C. The devices were attached to 1.57-mm thick FR-4 board with eutectic solder and the ball diameters and heights were in the range of 0.22 to 0.40 mm, and 0.16 to 0.25 mm, respectively. Both

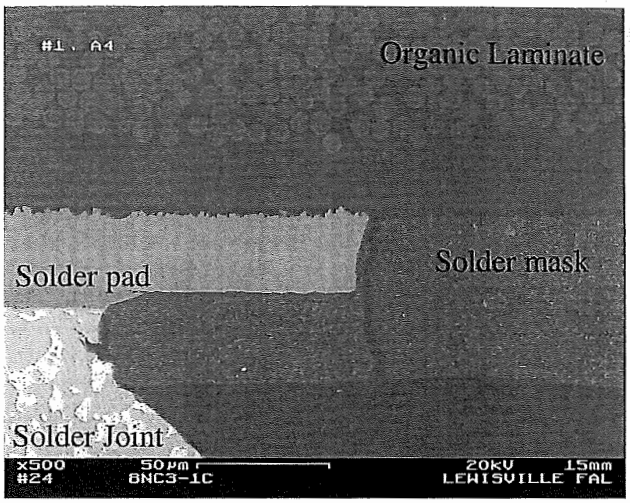


Fig. 18-41 Metallographic cross section showing a crack on the CSP side through the solder mask and up into the laminate carrier.

solder-mask defined and non-solder mask defined pads with OSP finish were employed. The two-parameter Weibull plots' summary for these packages indicated that the alpha ranged from 96 to 3690 and the beta values ranged from 2.68 to 93.5. This study suggests a considerable variation in board-level reliability, and that the general reliability of CSPs is lower than BGA packages whose ball pitch is considerably coarser [154,155]. Figure 18-43 shows the Weibull reliability plots of selected CSP packages and the variation in their reliabilities.

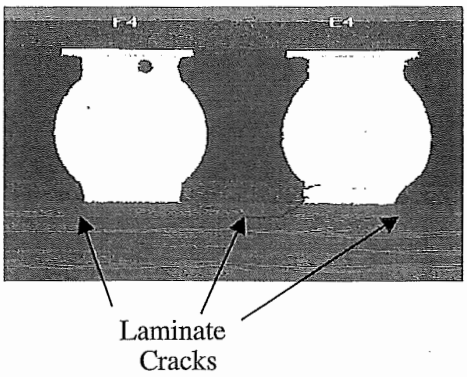


Fig. 18-42 Horizontal and vertical cracks in the FR4 board laminate after thermal cycling (−40 to 125°C). It is believed that contact of the high CTE solder mask with both solder joints constrained the x-y thermal growth resulting in a vertical force.

18.8.8 Reliability Comparisons

Caution needs to be exercised in comparing board-level reliability data of CSPs even if the investigations are carried out at the same stress levels/ranges and for the same type of packages. Considerable variations exist in Weibull plot beta values, time to first failures, etc.

18.8.8.1 Multiple factor variation There are numerous variables that can affect reliability making comparison of studies difficult. Some of the factors that influence board-level reliability are listed in Table 18-13.

(a) *Failure criteria*—Time to failure of course depends on the failure criteria, whether it is 10% resistance increase, a 20% change, a spike lasting a predetermined duration, or a complete electrical open. The failure criteria among studies reported in the literature vary, so direct comparisons are not always possible.

(b) *Thermal profile*—Differences in thermal profiles during testing such as rapid ramp rates (i.e., in excess of 15 deg/min) may

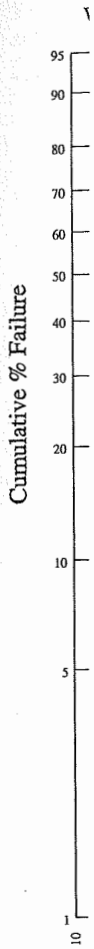


Fig. 18-
ball diar
MicroSy

induce
pared t
trans-g
Inadeq
leading
damag
laxing
ficient
ence b

(c) *I*
on bo

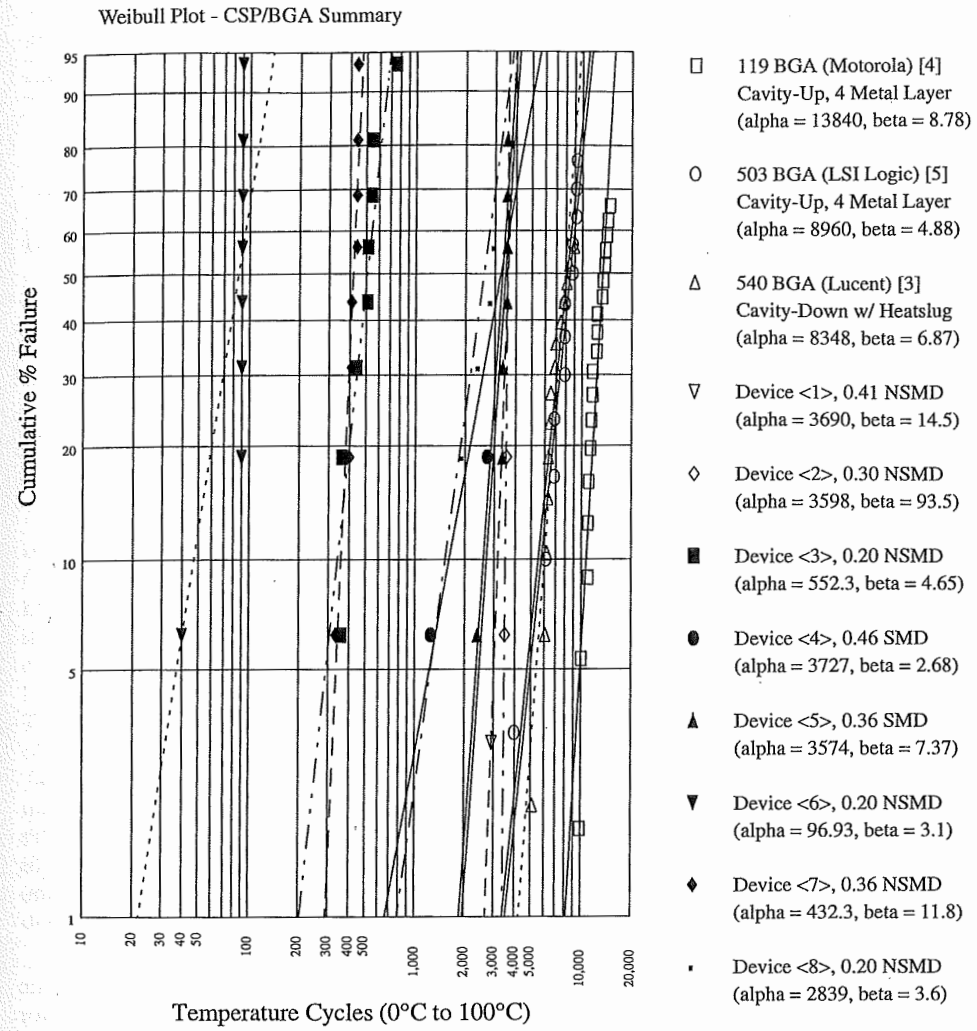


Fig. 18-43 Two parameter Weibull plots of selected CSPs with varying I/O counts, pitches, solder ball diameters, solder joint heights, and pad definitions. (Courtesy of K. Newman and M. Yuan of Sun MicroSystems).

induce a different failure mechanism compared to a lower ramp rate; an example is trans-granular versus inter-granular cracks. Inadequate dwell times can give rise to misleading results because the internal structural damage that the solder undergoes when relaxing during creep has not been given sufficient time to occur. Rapid test cycles influence both crack initiation and propagation.

(c) *Pad geometry*—Pad sizes and shapes on boards and packages also influence reliability. For example, pads with sharp corners are high-stress areas. A decrease of mounting pad diameter from 16 to 12 mils provides a 25% improvement in board level thermal cycling reliability at −40 to 125°C of 0.8 mm, 180 I/O chip scale packages [89]. Actual results will vary with solder volume.

(d) *Solder volume*—There are also competing factors; a fixed solder volume results in a slightly higher solder joint on

Table 18-13 Factors that have an effect on CSP solder joint reliability

Variable	Comment
Thermal profile; ramp-up, ramp-down, dwell at extremities	Intragranular vs. Intergranular with rapid ramp rates. Short dwells don't allow creep deformation.
Pad shapes	
Pad sizes	Larger pads generally improve reliability.
Solder volume	Increased volume generally improves reliability.
Pad definition—solder mask or non-solder mask defined	Conflicting opinions on which design offers best reliability.
Solder mask registration	Partial solder mask defined pads are less reliable.
Surface finish	Planar surfaces recommended as pitch decreases. Defects (porosity, black pad) cause poor wetting.
Solder alloy composition	Ductility and reflow processing temperatures vary between alloys.
Card structure—number of layers, material type	CTE varies with resin system, volume percent of Cu in PWB, and inclusion of low CTE materials.
Card thickness	Thin flexible boards can have improved CSP reliability.
Single sided or double sided assembly	Double sided boards are less flexible.
Mirrored placement or back to back components	Boards are less flexible.
Dummy solder balls	Added to corner locations on some CSPs.
Moisture sensitivity level rating of the packages	Lower reliability with increased moisture sensitivity.
Application environment	Reliability varies greatly depending on application environment (Δ Temp, shock, humidity, etc.).
Lifetime requirement	Number of power and thermal cycles, or expected years of service of each product alters the definition of "reliable".

a smaller pad when compared to a larger pad. While increasing joint height is a favorable reliability factor, a smaller pad also requires less time to propagate a crack through the joint. The relative effects of these and other parameters should be carefully evaluated in the context of specific product form factors and requirements. An optimization of the pad design based on solder volumes and the reliability requirements is desirable.

(e) *Flux vs. paste*—Table 18-14 shows a comparison of board-level reliability with flux-only and with paste assemblies [112]. Results indicate improved reliability when CSPs are attached using solder paste, which is due in part to increased solder volume.

(f) *Solder mask*—Solder joints on non-solder mask defined pads have been shown to offer a slightly greater reliability compared to those on solder mask defined pads [156]. Occasionally one encounters reports indicating either that there are no differences between the two or that joints on SMD pads are slightly better [156]. In such cases it is important to investigate other factors contributing to the discrepancy.

(g) *Solder composition*—While eutectic solder is the predominant solder alloy for board-level interconnections, the composition of the solder balls on the CSPs can significantly alter the solder joint behavior. Component solder balls often contain minute additions of elements such as Cu, Bi, Sb, Ag., etc. incorporated into the eutectic solder to enhance reliability. These alloys may not be compatible with the solder paste or the metallurgy of component and board terminations, further complicating reliability comparisons.

(h) *Card structure*—Card structure can also impact board-level reliability. Cards with embedded cores for thermal management may have a different local coefficient

Table 18-14 Comparison of board level reliability test results of the microStar™ BGA with only flux and with solder paste attachment process. (Courtesy Texas Instruments)

• *With solder paste*											
u*BGA™ Package	Body Size (mm)	Die Size (mm)	Mois. Soak (JEDEC)	Temp Cycle (°C)	0 cy	100	200	400	600	800	1000
144GGU (0.8 mm pitch)	12 × 12	8.8 × 8.8	2	−40/125	0/32	0/32	0/32	0/32	0/32	0/32	0/32
144GGU (0.8 mm pitch)	12 × 12	8.8 × 8.8	3	−40/125	0/36	0/36	0/36	0/36	0/36	0/36	0/36
• *Without solder paste*											
u*BGA™ Package	Body Size (mm)	Die Size (mm)	Mois. Soak (JEDEC)	Temp Cycle (°C)	0 cy	100	200	400	600	800	1000
144GGU (0.8 mm pitch)	12 × 12	8.8 × 8.8	6	−40/125	0/56	3/56	1/56	4/56	9/56	25/56	38/56

of thermal expansion compared to the global CTE. Thin cards generally are less rigid and hence offer a better thermal-cycling reliability compared to thicker cards. However, thin cards may perform worse under mechanical loading (shock, vibration, torque, etc.). Typical mechanical stress tests performed on consumer products are shown in Fig. 18-44. Thin cards when populated on both sides may act like thick cards due to added rigidity. All the above factors influence the assembly reliability so care must be exercised in making strict comparisons among studies cited in the literature. However, even with these variations, some trends have emerged. CSP reliability is discussed in more detail in Chapter 23.

18.8.9 *Assembly Guidelines to Optimize Reliability*

Based on industry experience and published work [101,102,103], the guidelines for board assembly of CSPs to enhance yield, throughput and reliability can be summarized as follows:

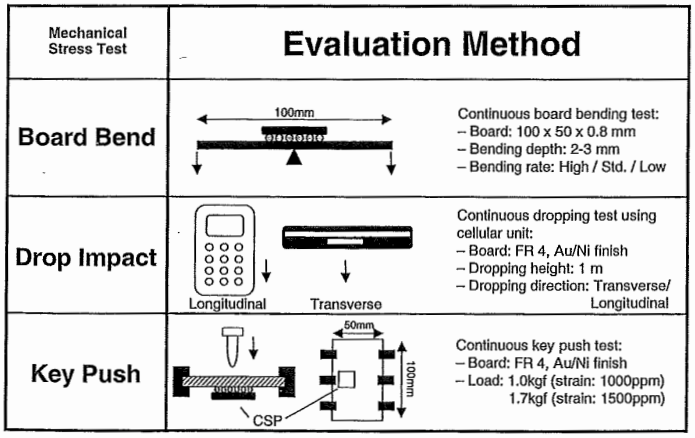


Fig. 18-44 Typical mechanical stress tests performed on consumer products.

- *Die size*—As die size decreases reliability increases for the same size of CSP.
- *Solder ball diameter*—As the solder ball diameter increases (taller the stand-off), reliability also increases, e.g., 0.45 mm is better than 0.35 mm diameter for 0.8 or 1.0 mm pitch CSPs.
- *Dummy solder balls*—on the four corners of a CSP can improve reliability (i.e., accelerated thermal cycling (ATC) test life).
- *Pad diameter on motherboard*—The smaller the pad diameter, the better the ATC reliability, e.g., 0.30 > 0.35 > 0.40 mm diameter for CSP48 with 0.45 mm diameter solder balls.
- *Board surface finish*—Electroless nickel with less than 2.3 microns immersion gold or organic solderability preservative (OSP) is an acceptable board surface finish; HASL (hot air solder leveling) can be an issue for CSPs with less than a 0.75 mm solder ball pitch.
- *CSP mounting position on motherboard*—From a reliability perspective a single-side board is the best, followed by the staggered two-sided board. The board with mirrored two-sided CSPs is the worst.
- *Mother board coefficient of thermal expansion (CTE)*—Lowering the CTE difference between the CSP substrate and mother board increases ATC reliability.
- *Board thickness*—A thin board increases ATC reliability but may have reduced reliability under mechanical loading (shock, vibe, torque, etc.); e.g., a 4-layer mother board is stiffer than a 2-layer one.
- *Others*—Back light (part outline only) is sufficient for pick and place; tape & reel is the preferred shipping medium; x-ray can be used for inspection of non-wet, shorts, and missing balls.

18.9 Other Key Enabling Technologies

18.9.1 Build-up Technology

For high-I/O, fine-pitch packages with small feature sizes one may be reaching the limits of the current printed wiring board technology in terms of providing requisite line widths, line spacing, via sizes, solder mask thickness, and precision and accuracy of registration. The need for microvia/redistribution layer technology is becoming increasingly apparent. CSPs, such as flexible and rigid-inter-poser type packages, require a high-density carrier technology to route all the connections from the package underside, especially for packages with a solder-ball pitch less than 0.75 mm [45]. Examples of commercially-available, high-density chip carriers are IBM's Surface Laminar Circuit (SLC)® and Hewlett-Packard's DYCO-strate® MCM-D/L technologies [157–163]. These and other build-up technologies are discussed in Chapter 7.

18.9.2 Test and Burn-in Capability

Test and burn-in of high-density CSPs [5] presents another challenge. With bare die it is difficult to make and maintain contact to small bond pads (<80 μm) on a tight pitch (~100 μm) over fairly large die-size areas during temperature excursions. CSP technology offers a relaxed pad pitch (no less than 0.5 mm) compared to bare die and therefore alleviates this problem to some extent, but does not eliminate burn-in and test difficulties. Improved techniques are needed.

18.9.2.1 Need test sockets/carriers The benefit of the relaxed pad pitch has not been realized, as there is no widely accepted, cost effective, socket available for array-type packages with pads or balls on pitches less than 1.0 mm. Several fine-pitch BGA sockets are available [94,95], but prices are relatively high (100s of US dollars) and their reliability is not well demonstrated. There has been a considerable effort within the industry to develop and evaluate temporary carriers for bare die, including solder-bumped. CSPs can potentially take advantage of these carrier developments. In addition, wafer-level test and burn-in related activities [164] can speed up the deployment of wafer-level processed CSPs.

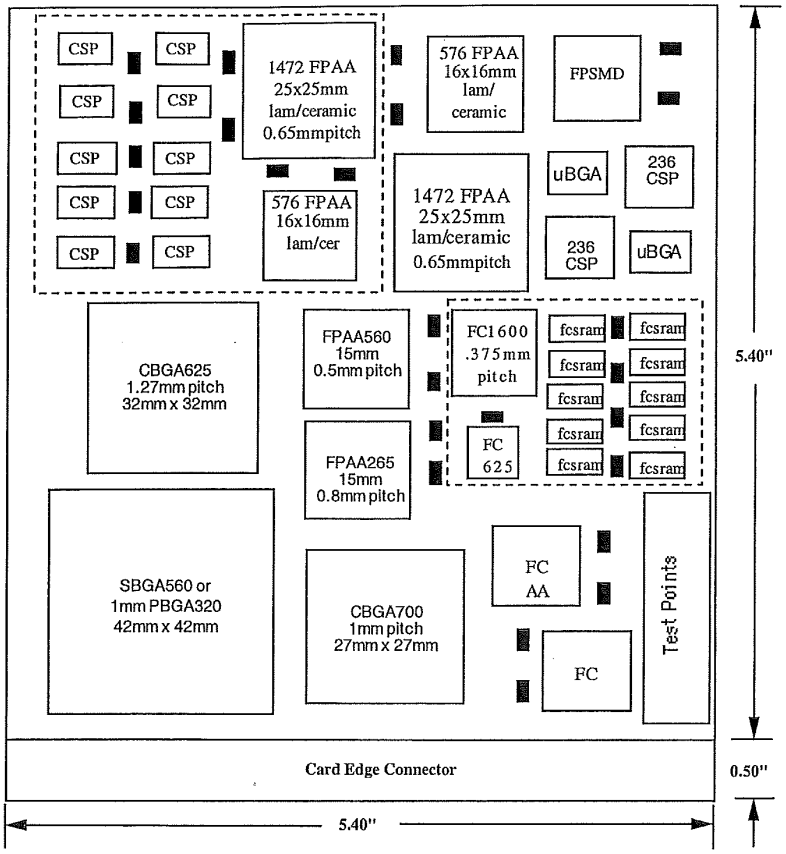


Fig. 18-45 Schematic drawing of a MCC fine pitch area-array test vehicle.

18.10 CSP Related Consortia Activities

There are a number of CSP-related consortia activities including those at Microelectronics and Computer Technology Corporation (MCC), Jet Propulsion Laboratory (JPL) [134, 165, 166], High-density Packaging Users Group (HDPUG), Universal Instruments [167], and IVF—The Swedish Institute of Production Engineering Research [168] investigating availability and board-assembly reliability of CSP. MCC is also addressing reliability of various CSPs on high-density carriers utilizing micro-vias, the electrical and thermal performance of CSPs and flip chips with up to 1600 chip I/O, and area-array package pitches down to a 0.65 mm. A schematic drawing of the MCC fine pitch, area-array test vehicle is shown in Fig. 18-45.

18.11 CSP Related Applications

Several types of CSPs have been implemented into a number of electronic products that require light weight and small size such as camcorders, personal digital assistants (PDAs), and cellular phones [4–9]. Some excellent examples follow.

- *Camcorder*—Sony Camcorder introduced a tiny liquid crystal display (LCD) Handycam (DCR-PC7) with a 6.25 cm built-in LCD monitor to the Japanese market in September 1996. The palm-sized camcorder measures 59 mm × 129 mm × 118 mm and weighs 500 grams (excluding the battery pack) making it the world's smallest and lightest consumer digital camcorder (with built-in LCD monitor). The

low weight and small size in part is due to utilizing 20 CSPs in the product, two of which are from TI Japan [53,57]. They are a 62-pin LSI image memory package (9 × 13 mm) and a 100-pin LSI communication analog package (10 × 10 mm). One NEC CSP is used, a 208-pin LSI control package (10 × 10 mm). All devices have a lead pitch of 0.5 mm. The remaining CSPs are believed to be assembled by Sony Device Manufacturing Division, which purchases bumped bare die from Sony Semiconductor Division and other semiconductor suppliers and assembles them into CSP packages. Sony CSPs used in their DCR-PC7 digital camcorder consist of IC peripheral I/Os, which are redistributed using Au/Cu/Cr wiring. Electrical connection is made between an area-bumped IC and an organic chip carrier with high-lead solder bumps. Since redistribution is handled at the die level, wiring requirements for organic chip carriers are not very severe (an advantage of this CSP structure). By choosing CSPs instead of 0.5 mm pitch QFPs, the required board area is reduced by almost 37%.

In addition, Sony's Assembly Division developed a CSP using a tape interposer, with an elastomer layer between the die and polyimide tape, which absorbs the stress to enhance reliability. Thermal cycle testing (−25 to 125°C, 1500 cycles) conducted on this CSP resulted in no failures [169].

- *Personal Digital Assistant*—Panasonic (PDA) utilized a CSP in their JT-SI palm-sized (136 × 93 × 19 mm) personal digital assistant, which incorporates a 4.6-inch mono-chrome touch panel LCD and weighs 220 grams. The CSP has gold-stud bumps formed on IC bond pads attached to a low-temperature, co-fired ceramic chip carrier (supplied by Kyocera) using conductive silver-palladium paste. The gap between the IC and chip carrier is filled with a sealing resin. The interconnection technology is well known in the industry as stud-bump bonding (SBB), which uses a conventional gold-wire bonder to form gold bumps individually on the IC bond pads. Solder paste is printed on the backside of a ceramic chip carrier and subsequently reflow attached to a board. Panasonic adopted the same SBB structure in the multi-chip module (MCM) used in its Pronote Jet Mini (a sub-notebook PC weighing 1.29 kg) introduced in 1995 and a single-chip CPU in Let's Note (a Pentium-based sub-notebook PC weighing 1.47 kg), offered in 1996.
- *Cellular Phones*—The Sharp Digital Cellular Phone SH201, made for NTT DoCoMo (a Personal Digital Cellular service provider), has four Sharp CSPs and one from TI Japan. This is the first digital cellular phone which utilized CSPs. The SH201 measures 105 × 60 × 20 mm and weighs 120 g. The four chip types used in the cellular phone are gate array, micro controller, flash memory, and SRAM, whose pin counts range from 28 to 128 pins. Sharp's CSP is similar to typical plastic packages with a single-layer of polyimide and copper pattern on one side. Sharp's CSPs have a gold-wire bond interconnection structure with array solder bumps on the backside of a polyimide interposer [132] and encapsulated with a transfer mold resin. Sharp offers a variety of CSPs with 0.8 mm or 1.0 mm pitch. Several Sharp product divisions and portable electronics manufacturers have adopted Sharp's CSPs into their respective products [8,102].

The Nokia 8810 GSM (Global System for Mobile Communications) cellular phone is another example of extensive use of chip scale packages and the utilization of microvia technology to enable the shrinkage of hand-held electronic equipment. It measures 107 cm × 46 cm × 18 cm, and contains six devices that are packaged in CSP format. The CSP types include wire-bonded packages on flex, wire bonded on rigid substrate, and TAB-tape-type packages. The package sizes range from 5 mm × 5 mm to up to 15 mm × 15 mm with I/O counts in the range of 48 to 176. Both full array and perimeter array interconnections are utilized. The carrier is a microvia substrate constructed

of a traditional PWB subcomposite core made of glass-filled epoxy layers with mechanically-drilled holes and plated-through holes. The top and bottom sides are laminated with a resin coated copper (RCC) to constitute the microvia layer. Microvias are formed on the RCC layer by laser ablation and then circuitized as required. The PWB is then coated with solder mask using conventional PWB practices. The microvias are 150 microns in diameter and the finished board is about 750 microns in thickness. The phone contains the radio section on the top half and digital base band section on the bottom half [170].

- *Others*—Both Panasonic and Sharp have produced Camcorders with CSPs [8]. Casio is developing CSP and flip chip technologies to be incorporated into future digital still cameras and other portable electronic devices in which the company specializes. Maxtor Corporation, a disk drive manufacturer, is evaluating the feasibility of incorporating a high I/O ASIC CSP package into a 2.5-inch drive [7].

18.12 Some Major Suppliers

A number of semiconductor manufacturers have either started or announced plans for volume supply of CSPs [4,9,11]. While most CSP suppliers are located in Japan such as Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, Sharp, and Toshiba, there are a number of U.S. companies such as 3M [171], AMD [4], Amkor [70], ChipScale [47], EPS [46,50,51], Intel [126,130], and Motorola [48,55,172], which are actively working on CSP-related projects or products. In addition to the references cited, more detailed information may be found in references [4,11,12].

18.13 New Developments

Although the wafer-level processed CSP (WLCSP) has not created a lot of market activities, it can be a very competitive approach for many applications especially for low-pin-count devices (less than 100). One of the major advantages of WLCSP is that it offers a complete packaging solution with the same form factor as solder flip-chip direct chip attach (DCA) without the requirement of underfill. Because processing is conducted at the wafer level, the potential cost saving can be substantial compared to singulated or die-level packages [173]. One example is the approach of wafer-pad redistributed demonstrated by Sandia's miniBGA made by Aptos (Fig. 18-20) [125, 131]. The approach represents a true die-size packaging solution since all the die pads are redistribution (fan-in) within the die area. The copper/polyimide-based redistribution technology illustrated by the cross-section in Fig. 18-20 was fabricated using mature thin-firm process with proven reliability. Excellent electrical perfomance is achieved due to the package profile, short lead length and controlled dimensions. The reliability performance of the package was also demonstrated as shown in Tables 18-11 and 18-12. In addition, the wafer-pad redistribution process can easily be integrated into IC front-end processes, reducing conventional IC packaging process steps; e.g., no die bonding, wire bonding or encapsulation. Other examples include Fujitsu's Super CSPs [56] and FCT's Ultra CSPs [174] which use large solder balls to provide extra solder joint height in order to alleviate the solder joint stress.

18.14 Future Developments

The need for high-density portable electronic hardware will continue in the new millennium. Higher I/O devices with lead counts in excess of 2000 are likely to be common place. High-density, multilayer-laminate technology for chip carrier as well as printed wiring board will be needed. Owing to an increased emphasis on environmental safety, the use of lead in electronic assemblies will be reduced and eventually eliminated. Alternative interconnection metallurgies will be explored. Also halide-free PWB materials will be incorporated.

18.14.1 SLC Micro-Via Board Construction

As one migrates from 0.8 mm pitch CSPs to 0.5 mm pitch packages conventional PWB technologies with mechanically-drilled vias do not satisfy the routing densities required to accommodate CSP assembly. High-density interconnect technologies for boards referred to as build-up technologies are making their way into mainstream products. They consist of organic carriers with via diameters of .15 mm (6-mils) or less made by non-mechanical methods, i.e., laser drilling, photo-imaging, or plasma.

18.14.2 Lead Free Solders

In recent years the electronics industry has witnessed an increased awareness on the potential health hazards of lead and efforts have been underway to decrease or eliminate lead in electronic assemblies. Elimination of lead implies exploration of new interconnection alloys that would take the place of the eutectic tin-lead alloy. A host of binary, ternary, and quaternary metallurgical compositions have been investigated. These include Sn/Bi, Sn/Ag/Cu, Sn/Ag/Cu/Bi, Sn/Ag, Sn/Ag/Cu/Sb, Sn/Ag/Cu/In, Sn/Zn, etc. Table 18-15 shows some of the likely compositions and the melting points of these alloys [175]. The Sn/Bi alloy has a lower melting point than eutectic Sn/Pb and may not meet the needs of the majority of electronic assemblies but may be useful for niche applications. Some compositions under investigation have significantly higher melting points.

Higher melting point alloys can have an effect on the integrity of current printed wiring boards, components, and packaging materials; impact assembly-process parameters; and ultimately affect product performance and reliability. Currently, there is no single drop-in replacement for eutectic Sn-Pb solder. Applications of Pb-free solders to chip scale package and assemblies have been reported in the literature. In case of CSPs compatibility between solder ball alloy, solder paste, and board finish is important. Watanabe and Ano have described

Table 18-15 Some Pb-free solder alloy compositions under consideration

Solder Alloy [177]	Approx. Weight %	Approx. Melting Temp. °C
Sn–Ag	Sn 98/Ag 2	220–226
Sn–Ag	Sn 96.5/Ag 3.5	221
Sn–Ag–Bi	Sn 90.5/Ag 2.0/Bi 7.5	207–212
Sn–Ag–Bi	Sn 91.8/Ag 3.4/Bi 4.8	208–215
Sn–Ag–Bi	Sn 93.5/Ag 3.5/Bi 3.0	206–213
Sn–Ag–Bi	Sn 95/Ag 3.0/Bi 2.0	220
Sn–Ag–Cu	Sn 96.3/Ag 3/Cu 0.7	217
Sn–Ag–Cu	Sn 93.6/Ag 4.7/Cu 1.7	218
Sn–Ag–Cu	Sn 95.5/Ag 0.5/Cu 4	260
Sn–Ag–Cu–Sb	Sn 96.2/Ag 2.5/Cu 0.8/Sb 0.5	213–218
Sn–Ag–Cu–Sb	Sn 96.7/Ag 2/Cu 0.8 /Sb 0.5	216–222
Sn–Ag–Cu–Zn	Sn 95/Ag 3.5/Cu 0.5/Zn 1.0	221
Sn–Ag–In	Sn 77.2/Ag 2.8/In 20	187
Sn–Bi	Sn 42/Bi 58	140
Sn–Cu	Sn 99.3/Cu 0.7	227
Sn–Sb	Sn 95/Sb 5	239
Sn–Zn	Sn 91/Zn 9	199
Sn–Zn–Bi	Sn 89/Zn 8/Bi 3	187–197

board-reliability results of Sn-Ag based alloys with minor element additions. Thermal cycle test results showed first fails in the vicinity of 1000 cycles (−40 to 125°C) [176]. In a related investigation of lead-free solders for flip chip applications Elenius demonstrated a proprietary alloy containing Sn/Ag/Cu/In alloy to yield more robust solder joints compared to Sn/Pb eutectic joints. Non-underfilled solder joints with the new alloy performed better than Sn/Pb joints by a factor of 1.5 when cycled from −50 to 150°C. Underfilled joints lasted in excess of 1500 cycles with no fails compared to 3 fails out of 40 samples in the case of Sn/Pb joints [177].

18.14.3 Alternative Board Materials

Halogenated fire retardants consist of a family of chemicals called polyhalogenated phenyl ethers. These class of compounds are incorporated into plastic materials to make them less flammable. However, it is alleged that when materials containing these compounds are disposed by incineration, they generate compounds such as dioxins, furans, etc., that are either known or suspected to be carcinogens. Boards used in electronic assemblies typically contain tetrabromobisphenol as a fire retardant. Other materials in this category are polybrominated bisphenols and polybrominated diphenyl ethers. The World Health Organization considers the risk to the general population from tetrabromobisphenol to be insignificant. However, there is a general emphasis on finding alternative safer material.

In addition to finding alternative flame retardants, emphasis on biodegradable materials for printed circuit boards is gaining ground. Materials based on proteins such as casein, carbohydrate materials such as cellulose and chitin are being explored.

18.15 Summary

In general, CSPs are more user-friendly than direct chip attach because CSPs are packaged components that can be tested and burned-in. CSPs can accommodate die shrinks resulting from improvements in silicon fabrication techniques while still offering a constant footprint to users. Flip chip on board or direct chip attach [51,162,178,179] is the ultimate choice for achieving the smallest possible footprint and the highest electrical performance, but CSPs can come close to the same performance at a lower risk. Future adaptation of high-I/O CSPs will be dependent on the availability of high-density chip carriers [163] at a reasonable cost. CSPs appear to offer the best combination of form factor, performance and ease-of-handling, as demonstrated by increasing product adoption of various types of CSPs by system manufacturers.

Wafer-level fabrication coupled with embedded encapsulant may blur the distinction between chip-scale packaging and flip-chip attach. It is anticipated that CSPs will become ever more prevalent with the development of improved organic laminates, better and reworkable underfill materials, and better design tools and test methodologies that can take into account chip and substrate complexities.

Acknowledgments

The authors express appreciation to Donal O'Connel and Kari Kulojarvi of Nokia for their encouragement and support as well as colleagues at APTOS Corporation, Dr. John Lau at EPS, Masako Robertson and Chris Windsor at MCC, Robert Champaign and Joe Colangelo at the Raytheon Failure Analysis Lab (FAL), Ted Carper at Nokia, Gary Morrison at Texas Instruments, Brian Czaplicki at Air-Vac Engineering, Ning-Cheng Lee at Indium Corp., Keith Newman and Mathew Yuan at Sun MicroSystems, Dr. Yu-Wen Huang at the Singapore Institute of Microelectronics, and Dr. Rajan Chanchani at Sandia for providing information for this chapter.

Suggested Reading

Solder Joint Reliability of BGA, CSP, and Flip Chip, ed. J. H. Lau, McGraw Hill Book, Inc., New York, N.Y. 1998.

Chip Scale package, Design, Materials, Process, Reliability and Applications, J. H. Lau and A. W. Rickey Lee, McGraw Hill Book, 1999.

References

1. R. Tummala et al., *Microelectronic Packaging Handbook*, New York: Chapman & Hall, 1997.
2. T. Chung et al., "Trends in Microelectronics and Packaging Interconnection," *Proceedings of IEEE Japan International Electronics Manufacturing Technology Symposium*, pp. 27–31, Dec. 1995.
3. G. Mukarami, "Package Industry, Roadmap to the Future," *Proceedings Semicon West* 1994.
4. A CSP article (in Japanese), *Nikkei Electronics*, pp. 139–145, Aug. 1996.
5. L. Gilg and T. Chung, "Known Good Die versus Chip Size Package: Options, Availability, Manufacturability, and Reliability," *Proceedings of the SMI Conference*, San Jose, CA, pp. 244–250, 1996.
6. K. Fujita, "CSP Packages Get Skintight," *Nikkei Electronics Asia*, pp. 52–54, Apr. 1995.
7. B. Rugg, "Pilot Assembly Results with a BGA Chip Scale Package," *Proceedings of the SMI Conference*, San Jose, CA, pp. 256–259, 1996.
8. M. Robertson, "Overview of Packaging Trends in Recent Japanese Portable Electronics," *NEPCON-East 1997*, pp. 121–131.
9. Nikkei Microdevices, Feb. 1998, pp. 40–47.
10. K. Nakajima, "CSP Primer for Original Equipment Manufacturers," *Chip Scale Review*, Volume 2(4): pp. 58–61, Sept. 1998.
11. T. Chung et al., "Updates on Worldwide Chip Scale Packaging," *The 2nd International Conference on Chip Scale Packaging*, Feb. 1997.
12. T. Chung et al., "Updates on Worldwide Chip Scale Packaging (II)," *Proceedings of the Chip Scale Packaging Symposium, SMI*, San Jose, CA, pp. 1–11, Sept. 1997.
13. Joint Industry Standard J-STD-012, "Implementation of Flip Chip and Chip Scale Technology," Jan. 1996, p. 1.
14. J. Baliga, "Defining the CSP," *Chip Scale Technology, Special Supplement to EP&P and Semi Conductor International*, pp. 6–8, Sept. 1999.
15. J. Baliga, "The High Pin Count Workhorse," *Semiconductor International*, pp. 81–87, Sept. 1999.
16. J. L. Young, "Chip-Scale Packaging," *Advanced Packaging*, pp. 26–29, Jan./Feb. 1996.
17. J. Young, "Micro SMT Packaging," *Technical Paper by ChipScale, Inc.*, Sept. 1996.
18. J. Kasai, "Low Cost Chip Scale Package for Memory Products," *Proceedings of the SMI Conference*, San Jose, CA, pp. 6–17, 1995.
19. J. Kasai, "Low Cost Chip Size Package Solutions for Memory Application," *Technical Programs of SEMICON West*, pp. 5–29, 1996.
20. N. Taketani et al., "CSP with LOC Technology," *ISHM 1996 Proceedings*, pp. 594–599.
21. G. Forman et al., "Developments of GE's Plastic Thin-Zero Outline Package (TZOP) Technology," *Proceedings of IEEE Electronic Components & Technology Conference*, pp. 664–668, May 1995.
22. R. Master et al., "Ceramic Mini-Ball Grid Array Package for High Speed Device," *Proceedings of IEEE Electronic Components & Technology Conference*, pp. 46–50, May 1995.
23. K. Cha et al., "Ultra-thin & Crack-Free Bottom Leaded Plastic (BLP) Package Design," *Proceedings of IEEE Electronic Components & Technology Conference*, pp. 224–228, 1995.
24. Y. Kim et al., "Bottom Leaded Plastic (BLP) Package: A New Design with Enhanced Solder Joint Reliability," *Proceedings of IEEE Electronic Components & Technology Conference*, pp. 448–452, May 1996.
25. Y. Kim et al., "New Infrastructure for the BLP Package and Solder Joint Reliability," *Technical Programs of SEMICON West*, pp. 39–45, 1996.
26. Y. Kunitomo et al., "CSP (Chip Size

Package)," *Proceedings of 2nd VLSI Packaging Workshop*, pp. 51–56, Nov. 1994.

27. Y. Bessho et al., "A Stud-Bump-Bonding Technique for High Density Multichip Module," *Proceedings of IEEE International Electronics Manufacturing Technology Symposium*, pp. 362–365, 1995.
28. Y. Kunitomo, "Practical Chip Size Package Realized by Ceramic LGA Substrate and SBB Technology," *Proceedings of the SMI Conference*, pp. 18–25, 1995.
29. M. Yasunaga et al., "Chip Scale Package (CSP): A Lightly Dressed LSI Chip," *Proceedings of IEEE International Electronics Manufacturing Technology Symposium*, pp. 169–176, Sept. 1994.
30. M. Matsuo et al., "Smallest Flip-Chip-Like Package: Chip Scale Package (CSP)," *Proceedings of 2nd VLSI Packaging Workshop*, pp. 46–50, Nov. 1994.
31. S. Baba et al., "Molded Chip Scale Package for High Pin Count," *Proceedings of IEEE Electronic Components & Technology Conference*, pp. 1251–1257, May 1996.
32. K. Banerji, "Development of the Slightly Larger Than IC Carrier (SLICC)," *Proceedings of NEPCON West*, Feb. 1994, pp. 1249–1256.
33. K. Banerji et al., "Development of the SLICC Package," *Proceedings of NEPCON East*, pp. 441–451, June 1995.
34. P. Lall et al., "Reliability Characterization of the SLICC Package," *Proceedings of IEEE Electronic Components & Technology Conference*, pp. 1202–1210, May 1996.
35. S. Matsuda et al., "Simple-Structure, Generally Applicable Chip-Scale Package," *Proceedings of IEEE Electronic Components & Technology Conference*, pp. 218–223, May 1995.
36. S. Tanigawa et al., "The Resin Molded Chip Size Package (MCSP)," *Proceedings of IEEE International Electronics Manufacturing Technology Symposium*, pp. 410–415, Oct. 1995.
37. R. Chanchani, K. Treece and P. Dressendorfer, "Mini Ball Grid Array Technology," *Proceedings of the NEPCON West'95*, Anaheim, CA, pp. 938–945, 1995.
38. A. Badihi et al., "ShellCase—A True Miniature Integrated Circuit Package," *Proceedings of Flip Chip, BGA, TAB, and Advanced Packaging Symposium*, pp. 244–252, Feb. 1995.
39. G. Zilber et al., "ShellPACK—A Thin Chip Size, Integrated Circuit Package," *Technical Programs of SEMICON West*, pp. 31–36, 1996.
40. T. Koyama et al., "Reliability of mBGA Mounted on a Printed Circuit Board," *Proceedings of SMI Conference*, pp. 43–56, Aug. 1995.
41. V. Solberg, "Chip-Scale Ball Grid Array Packaging for Surface Mount Technology," *Proceedings of SMI Conference*, pp. 221–228, 1996.
42. J. Fjelstad et al., "Compliancy Modeling of an Area Array Chip Scale Package," *Proceedings of SMI Conference*, pp. 236–243, 1996.
43. M. Momma, "Update CSP Development of BGA/LGA Type," *Proceedings of the 4th Surface Mounting Technology Forum*, Oct. 4, 1996.
44. H. Iwasaki, "CSTP: Chip Scale Thin Package," *Proceedings of SEMICON Japan*, pp. 488–495, Nov. 1994.
45. C. Takubo et al., "Eutectic Solder Flip Chip Technology for Chip Scale Package," *Proceedings of IEEE International Electronics Manufacturing Technology Symposium*, pp. 488–493, Oct. 1996.
46. T. Chou et al., " A Low-Cost Chip Size Package—NuCSP," *NEPCON West*, Feb. 1997.
47. J. Young, "Designing Wafer Level Chip Scale Packages to JEDEC and EIAJ Outlines," *NEPCON-West*, Feb. 1997.
48. J. Aday, C. Koehler and T. Tessier, "A Laminate-Based Flip-Chip Chip Scale Package," *Proceedings of the Chip Scale Packaging Symposium, SMI*, pp. 12–16, Sept. 1997.
49. M. Amagai et al., "Development of Chip Scale Packages (CSP) for Center Pad Devices," *Proceedings of the 47th ECTC*, pp. 343–352, May 1997.
50. J. H. Lau, "Solder Joint Reliability of a Low Cost Chip Size Package—NuCSP," *Proceedings of ISHM Microelectronics Symposium*, pp. 691–696, Oct. 1997.
51. J. H. Lau et al., "A Low-Cost Solder-Bumped Chip Scale Package—NuCSP," *Proceedings of the NEPCON WEST*, Mar. 1998.
52. J. Link et al., "Placement and Reflow of 0.3 mm Diameter Solder Balls for

Chip-Scale BGA Devices," *Proceedings of the Chip Scale Packaging Symposium, SMI*, San Jose, CA, pp. 17–22, Sept. 1997.

53. K. Ano et al., "Reliability Study of the Chip Scale Package Using Flex Substrate," *Proceedings of the Chip Scale Packaging Symposium, SMI*, San Jose, CA, pp. 17–22, Sept. 1997.
54. R. Fillion et al., "Chip Scale Packaging Using Chip-on-Flex Technology," *Proceedings of the 47th ECTC*, pp. 638–642, May 1997.
55. S. Lindsey et al., "JACS-Pak Flip-Chip Chip Scale Package Development and Characterization," *Proceedings of the 48th ECTC*, pp. 511–517, May 1998.
56. M. Hou, "Super CSP: The Wafer Level Package," *Proceedings of the SEMICON West*, pp. F1–F10, July 1998.
57. M. Watanabe et al., "The Reliability Study of Lead-Free Solder Ball for the Chip Scale Package (CSP)," *Proceedings of the SMI Conference*, San Jose, CA, pp. 233–237, Sept. 1998.
58. P. Lall et al., "Assembly-Level Reliability of Flex-Substrate BGA, Elastomer-on-Flex Packages and 0.5 mm Pitch Partial Array Packages," *Proceedings of the SMI Conference*, San Jose, CA, pp. 238–255, Sept. 1998.
59. J. Lau et al., "Low-Cost Solder-Bumped Chip Scale Package," *Electronic Packaging & Production*: pp. 74–78, Nov. 1998.
60. J. Clech et al., "Reliability Prediction Modeling of Area Array CSPs," *Electronic Packaging & Production*, pp. 91–96, June 1997.
61. C. Windsor et al., "An Introduction to Chip Scale Package Technology," *Proceedings of NEPCON West*, pp. 1005–1012, 1996.
62. Z. P. Wang, D. J. Xie and K. M. Chua, "Interconnect Design and Reliability of Land Grid Array CSPs," *Proceedings of the Third Annual CSP Symposium, SMI*, San Jose, CA, pp. 69–76, Sept. 1999.
63. K. Cha, Y. G. Kim and T. K. Kang, "Ultra-Thin and Crack Free Bottom Leaded Plastic (BLP) Package Design," *Proceedings of the 45th ECTC*, Las Vegas, NV, pp. 224–228, May 1995.
64. N. Taketani, K. Hatano, H. Sujimoto and G. Mukarami, "CSP with LOC Technology" *Proceedings of the ISHM International Symposium on Microelectronics*, Minneapolis, MN, pp. 594–599, Oct. 1996.
65. G. Mukarami, "Rationale for Chip Scale Packages rather than Multi-Chip Modules (MCM)," *Proceedings of SMI Conference*, San Jose, CA, pp. 1–5, Aug. 1995.
66. K. Banerjee and P. Lall, "Development of the SLICC package," *Proceedings of the NEPCON East Conference*, Boston, MA, pp. 441–451, June 1995.
67. Y. Kim, D. Kim and K. Korea, "QFN Packaging Technology for CSPs," *Proceedings of the 1998 Pan pacific Microelectronics Symposium*, Mauna Lani, Hawaii, pp. 57–62, Feb. 1998.
68. R. N. Master, R. Jackson, S. K. Ray and A. Inghram, "Ceramic Ball Grid Array Package for High Speed Device," *Proceedings of the 45th ECTC*, Las Vegas, NV, pp. 46–50, May 1995.
69. S. Uegaki, S. Matsuzono, S. Sato, T. Kubota, Y. Basho and S. Matsuda, "Broadening the Ceramic CSP market for Higher Reliability Applications," *Proceedings of the Third Annual CSP Symposium*, San Jose, CA, pp. 29–36, Sept. 1999.
70. J. H. Lau and S. W. R. Lee, *Chip Scale Package (CSP)—Design, Materials, Process, Reliability, and Applications*, McGraw-Hill, 1999, pp. 439, chapters 3,5,12,19,22, chapter 28.
71. T. DeStefano, "The μBGA as a Chip Size Package," *Proceedings of NEPCON West*, Anaheim, CA, pp. 327–333, 1995.
72. K. Ano, T. Ouchida, K. Murata and M. Watanabe, "Reliability Study of the Chip Scale Package using Flex Substrate," *Proceedings of the Chip Scale Packaging Symposium, SMI Conference*, San Jose, CA, pp. 44–47, 1997.
73. R. D. Schuller, Enhanced Flex Based CSPs, *Proceedings of the Technical Program of NEPCON West*, Anaheim, CA, 1999.
74. R. Schueller et al., "Flex-Based Chip-Scale Packages," *Chip Scale Review*, Volume 3, Number 1: pp. 37–43, Feb. 1999.
75. R. J. Wounarowski and R. A. Fillion, "General Electric Floating Pad Technology™ For BGA and Other Mismatched CTE Interfaces," *Proceedings of the Chip Scale Packaging Symposium, SMTA International*, San Jose, CA, Sept. 12–16, 1999.
76. ViaThin™ Design Guidelines," http://www.sheldahl.com, Longmont, CO.

77. T. H. DeStefano, "Wafer Level Fabrication of IC Packages," *Chip Scale Review* vol. 1, no. 1: pp. 20–27, May 1997.

78. "A New Mini Ball Grid Array Multi Chip Module Technology," *International Journal of Microcircuits and Electronic Packaging*, vol. 18, no. 3: pp. 185–192, 1995.

79. M. Hou, "Super CSP: The Wafer Level Package," *Proceedings of Semicon West*, San Jose, CA, pp. F1–10, July 1998.

80. M. Hou, "Wafer level Packaging for CSPs," *Semiconductor International*, vol. 21, no. 8: pp. 305–308, July 1998.

81. P. Elenius and H. Yang, "The Ultra CSP Wafer Level Package," *High Density Interconnect*: pp. 36–39, Oct. 1998.

82. P. Elenius and H. Yang, "The Ultra CSP Wafer Scale Package," *Circuits Assembly*, vol. 10, no. 2: pp. 48–57, Feb. 1999.

83. J. Fjelstad, "WAVE Technology and Wafer Level Packaging of ICs," *http://www.tessera.com*, San Jose, CA.

84. T. Hamano, E. Sakota and S. Maki, "Enhanced BCC++™ Package for RF Devices," *Proceedings of the CSP Symposium*, San Jose, CA, pp. 1–6, Sept. 12–16, 1999.

85. T. Hamano, E. Sakota and S. Maki, "Enhanced BCC ++™ Package for RF Devices," *Proceedings of the Chip Scale Packaging Symposium*, San Jose, CA, pp. 1–6, Sept. 1999.

86. A. Badihi et al., "ShellCase—A True Miniature Integrated Circuit Package," *Proceedings of Flip Chip, BGA, TAB, and Advanced Packaging Symposium*, pp. 244–252, Feb. 1995.

87. V. Solberg, "JEDEC/EIAJ Standards for Chip-Scale Packaging," *Chip Scale International Conference*, May 1997.

88. "JEDEC JC-11 committee, JEDEC publication 95 and EIA publication PDP-100," *http://www.JEDEC.org.*

89. A. Primavera, "Influence of PCB parameters on CSP Assembly and Reliability (Part I)," *Proceedings of CSP Symposium, SMTA International*, San Jose, CA, pp. 97–109, Sept. 12–16, 1999.

90. A. Mawer, "Array Packaging Attachment Reliability, Paper#6," *Proceedings of the 7th Annual Electronics Packaging Symposium*, SUNY, Binghamton, NY, June 27–28, 1996.

91. P. Viswanadham, S. O. Dunford and T. Carper, "Board Level Reliability Evaluations of 40, 32 and 30 Mil Pitch Ball Grid Array Packages Over −40 to 125°C," *Pan Pacific Microelectronics Symposium*, Kauai, Hawaii, pp. 362–375, Feb. 2–5, 1999.

92. M. Avery, L. Gopalakrishnan and R. Srivastava, "Interconnect Reliability of Micro BGA and Chip Scale Packages," *Proceedings of Pan Pacific Microelectronics Symposium*, Kauai, Hawaii, pp. 71–78, Feb. 2–5, 1999.

93. J. Partridge and C. Hart, "Taking the CSP Plunge," *Electronic Packaging and Production*, pp. 48–53, Apr. 1999.

94. J. Glazer, P. A. Kramer and J. W. Morris Jr., "Effect of Au on the Reliability of Fine Pitch Surface Mount Solder Joints," *Journal of Surface Mount Technology*, pp. 15–27, Oct. 1999.

95. E. E. Benedetto, "Solderability and Board Level Reliability of Palladium Plated, Fine Pitch Components," *Proceedings of Surface Mount International*, pp. 624–631, Aug. 1998.

96. M. Watanabe and K. Ano, "Solder Joint Study of CSP For Use During the Transition Period to Lead Free Process," *Proceedings of CSP Symposium*, San Jose, CA, pp. 12–19, Sept. 12–16, 1999.

97. IPC TM 650.

98. R. Black et al., "The Impact of Chip Scale Pack-ages on the SMT Assembly Process," *Proceedings of SMI*, San Jose, CA, pp. 253–255, 1996.

99. K. Ano et al., "Reliability Study of the Chip Scale Package using Flex Substrate," *Proceedings of the CSP Symposium, SMI*, San Jose, CA, pp. 44–47, Sept. 1997.

100. R. Evans et al., "Implementation of Area Array, Chip Scale Packages, Ball Grid Arrays, and Ultra-Fine Pitch Devices," *Future Circuits International*, Issue 1, Volume 2: pp. 51–55, 1997.

101. J. Partridge et al., "Influence of Process Variables on the Reliability of MicroBGA Package Assemblies," *Proceedings of the 48th ECTC*, pp. 518–524, May 1998.

102. H. Juso et al., "Board Level Reliability of CSP," *Proceedings of the 48th ECTC*, pp. 525–531, May 1998.

103. I. Sterian et al., "Compatibility of CSPs in SMT Assembly," *Proceedings of the SMI*

Conference, San Jose, CA, pp. 225–230, Sept. 1998.

104. S. O. Dunford, P. Viswanadham and C. Clark, "Enhancing Board Level BGA Assembly and Reliability," *Proceedings of the 1999 SMTA International Conference Technical Program*, San Jose, CA, pp. 76–96, Sept. 1999.
105. A. Chen, K. Chang, N. Romas, J. Bragg, C. Quan and R. Ghaffarian, "Manufacturing Robustness of CSP on SMT Line," *Proceedings of the Third Annual CSP Symposium*, San Jose, CA, pp. 29–36, Sept. 1999.
106. S. Yi, R. Bhat, A. Lewis and K. Nakajuma, "Solder Paste Printing Optimization For CSP," *Proceedings of SMTA International*, San Jose, CA, pp. 11–16, Sept. 1999.
107. S. Yi, R. Bhat, A. Lewis and K. Nakajuma, "Optimizing Assembly Process for Newer Generation of CSPs," *Real World BGA/CSP Applications, SMTA, NEPCON Texas*, Dallas, TX, Oct. 1999.
108. S. C. Hung, P. Y. Zheng, H. N. Chen, S. C. Lee and J. J. Lee, "Board Level Reliability of Chip Scale Packages," *Proceedings, IMAPS International Symposium on Microelectronics*, Chicago, IL, pp. 571–580, Oct. 26–28, 1999.
109. V. Solberg, "Solder Stencil Requirement for μBGA," Technical Info, Application Notes.
110. N. C. Lee and W. Casey, "Soldering Technology for Area Array Packages," *Proceedings of Real World BGA/CSP Applications, SMTA, NEPCON Texas*, Dallas, TX, pp. 22–36, Oct. 1999.
111. J. Kennedy and J. Ros, "Solder Paste Requirements for CSP Packages," *Proceedings of the 1999 SMTA International Conference Technical Program*. San Jose, CA, pp. 58–65, Sept. 1999.
112. G. Morrison and L. Stark, "Chip Scale Package Design for Reliability, Texas Instrument's MicroStar BGA™ Board Level Reliability," Feb. 14, 1998. Presentation at Dallas SMTA, Monthly Meeting.
113. R. Noreika, C. Fieselman, K. Slesinger and M. Wells, "SMT Component Self-Centering Properties During Solder Reflow," *Proceedings of SMI*, San Jose, CA, pp. 338–346, Sept. 1997.
114. G. Schiebel, "High Speed Second Level CSP and Flip Chip Assembly Using Flip Chip Shooters," *Proceedings of SMTA International Conference Technical Program*, San Jose, CA, pp. 108–115. Sept. 1999.
115. A. Primavera, R. Sturm, S. Prasad and K. Srihari, "Factors that Affect Void Formation," *Journal of Surface Mount Technology*, vol. 12, no. 1: pp. 19–26, 1999.
116. A. DerMerderosian and V. Gonet, "The Effect of Entrapped Bubbles in Solder Used for Attachment of Leadless Ceramic Chip Carriers," *IEEE/IRPS Publication*, pp. 235–241, Boston, Mass., 1983.
117. R. J. K. Wassink, "Soldering in Electronics, 2nd edition," *Electrochemical Publishing*, Ltd. Ayr, Scotland, 1989.
118. D. R. Banks, T. E. Burnette, Y. C. Cho, W. T. DeMarco and A. J. Mawer, "The Effect of Solder joint Voiding on Plastic BGA Reliability," *Proceedings of the SMI Conference*, San Jose CA, pp. 121–126, 1996.
119. P. Wood, "Solder Paste Deposition in BGA and CSP Rework," *Proceedings of the 1999 Surface Mount Technology Association-International Conference Technical Program*, San Jose, CA, pp. 243–248, Sept. 1999.
120. T. Chung et al., "Rework of Ball Grid Array Assemblies," *NEPCON West*, Anaheim, CA, pp. 334–345, Feb. 1995.
121. J. H. Lau, *Ball Grid Array Technology*, McGraw-Hill, 1995, pp. 491–516.
122. C. Windsor et al., "Reworking Chip Scale Packages," *Proceedings of the Chip Scale Packaging Symposium, SMI*, Sept. 1997, pp. 55–62.
123. P. Wood, "A Successful Rework Process for Chip-Scale Packages," *Chip Scale Review*, Volume 2(4): pp. 41–45, Sept. 1998.
124. R. Aguirre, "BGA Rework In A Low Volume, High Mix Environment," *Proceedings of Real World BGA/CSP Applications*, SMTA/NEPCON Dallas, Dallas, TX, pp. 38–44, Oct. 27, 1999.
125. R. Chanchani et al., "Mini Ball Grid Array (mBGA) Technology," *Proceedings of NEPCON West*, Anaheim, CA, Feb. 1995, pp. 938–945.
126. S. Greathouse, "Critical Issues with Chip Scale Packages (CSPs)," *SMI Conference Proceedings*, pp. 203–215, 1996.
127. J. Lau and Y. Pao, "Solder Joint Reliability of

BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies," McGraw-Hill, 1997.

128. J. Lau et al., "Temperature-Dependent Elasto-Plastic-Creep Analysis of a Chip Scale Package's Solder Joint," *ASME Winter Annual Meeting*, Nov. 1996.
129. V. Solberg, "Qualification Test Planning for Chip-Scale and Chip-Size BGA Devices," SMTA Proceedings, pp. 117–123, Apr. 1997.
130. S. Greathouse, "Qualification Testing of Chip Scale Packages," *Chip Scale International Conference*, May 1997.
131. R. Chanchani et al., "Mini Ball Grid Array (mBGA) Assembly on MCM-L Boards," *ECTC*, May 1997, pp. 656–663.
132. Y. Yamaji et al., "Development of Highly Reliable CSP," *ECTC*, pp. 1022–1028, May 1997.
133. Y. Kim, "Solder Joint Reliability of Leaded and Leadless Packages: New BLP Design," *SEMICON West*, July 1997.
134. R. Ghaffarian et al., "Reliability of BGA Packages for Highly Reliable Applications and Chip Scale Package Board Level Reliability," *Proceedings of the Chip Scale Packaging Symposium, SMI*, San Jose, CA, pp. 48–54, Sept. 1997.
135. S. Uegaki et al., "Ceramic CSP—Current Status of Technology," *Proceedings of the SMI Conference*, San Jose, CA, pp. 179–186, Sept. 1998.
136. Y. Kim et al., "Solder Joint Reliability of a New, Leadless CSP," *Chip Scale Review*, Volume 1(4), pp. 46–54, Dec. 1997.
137. R. Ghaffarian, "Joint Integrity of Chip-Scale Packages Under Isothermal Aging," *Chip Scale Review*, Volume 2(3): pp. 74–78, July 1998.
138. L. Nguyen et al., "Wafer Level Chip Scale Packaging—Solder Joint Reliability," *Proceedings of the 1998 International Symposium on Microelectronics*, pp. 868–875, Nov. 1998.
139. R. Gannamani, V. Valluri, Sidharth and M. Zhang, "Reliability Evaluations of Chip Scale Packages," *Proceedings of the Chip Scale Packaging Symposium*, San Jose, CA, pp. 116–121, Sept. 12–16, 1999.
140. A. Primavera, "Influence of PCB Parameters on Chip Scale Package Assembly and Reliability (Part II)," *Proceedings of CSP Symposium*, San Jose, CA, pp. 97–109, Sept. 12–16, 1999.
141. R. Ghaffarian, "Chip Scale package and assembly Joint Reliability," *Proceedings of the Technical Program of 1999 NEPCON West Conference*, Anaheim, CA, Sept. 1999.
142. R. Ghaffarian, "CSP Assembly Reliability," *Circuits Assembly*, vol. 9, No. 9: pp. 36–42, Sept. 1998.
143. Intel, *Micro BGA Application Notes, http://www.intel.com.*
144. F. Cordes and R. Huemoeller, "Electroless Nickel-Gold: Is There A Future?," *Future Circuits International*, Issue 4: pp. 131–134, Nov. 1998.
145. F. D. Bruce Houghton, "'Solving the ENIG Black Pad Problem,' An ITRI Report on Round II," *Proceedings of International Summit on Pb Free Solders*, pp. S-04-3-1, Oct. 23–28, 1999.
146. K. Putlitz, "Preparation, Structure, and Fracture Modes of Pb-Sn, Pb-In terminated Flip Chip Attached to Gold Capped Microsockets," *IEEE TransCHMT*, vol. 13, pp. 647–655, 1990.
147. E. Bradley and K. Banerjee, "Effects of PCB finish on the reliability of BGA Packages," *ECTC Conference Proceedings*, Las Vegas, NV, pp. 1028–1030, May 1995.
148. Z. Mei, P. Callery, D. Fisher, F. Hua and J. Glazer, "Interfacial Fracture Mechanism of BGA Packages on Electroless Ni/Au," *Advances in Electronic Packaging*, EEP-Vol. 19-2, 1997.
149. N. Biunno, "A Root Cause Failure Mechanism For Solder Joint Integrity of Electroless Ni/Immersion Gold Surface Finishes," *Proceedings of the SMTA-I Technical Program*, San Jose, CA, pp. 561–568, Sept. 1999.
150. W. Casey, Reduction of BGA Eutectic Ball Solder Joint Voiding," *Proceedings of the Technical Program of SMI*, San Jose, CA, pp. 541–548, Sept. 1998.
151. D. R. Banks, R. Burnette, C. Chow, W. T. DeMarco and A. Mawer, "The Effects of Solder Joint Voiding on PBGA Reliability," *Proceedings of the Technical Program*, SMI, San Jose, CA, Aug. 1996, pp. 121–126.
152. D. Miller, "Inspection Criteria for Ball Grid Arrays," *Evaluation Engineering*, vol. 38, #9, pp. 128–143, 1999.
153. Y. W. Huang, K. H. Teo, K. L. Chua, M. W. R.

Yang and W. Ferns, "The Effect of Underfill on the Pressure Cooker Test Performance of Flip Chip on Board Assembly," *Advances in Electronic packaging—1999*, vol. 26-2: pp. 1121–1127, ASME, 1999.

154. K. Neuman and M. Yuan, "Board Level Evaluations of Various Chip Scale Packages," *Proceedings of the Technical Conference at Chip Scale International*, San Jose, CA, pp. 99–113, Sept. 1998.
155. T. Thompson, A. Carrasco and A. Mawer, "Reliability Assessment of Thin (Flex) BGA Using a Polyimide Tape Substrate," *Proceedings of SMTA International Conference Technical Program*, San Jose, CA, pp. 195–201, Sept. 1999.
156. P. Virpi, T. Markku, R. Tommi, Z. Jiansen and L. Wei, "TBGA Reliability in Telecom Environment," *Proceedings of SMTA International Conference Technical Program*, San Jose, CA, pp. 221–228, Sept. 12–16, 1999.
157. Y. Tsukada et al., "Surface Laminar Circuit Packaging," *Proceedings of the 42nd IEEE Electronic Component and Technology Conference*, pp. 22–27, May 1992.
158. D. Carey et al., "MCM-L Substrates for a 300 MHz Workstation," *The ISHM International Journal of Microcircuits & Electronic Packaging*, Volume 18: (4), pp. 454–458, 4th quarter, 1995.
159. H. Holden, "Comparing Costs for Various PWB Build-Up Technologies," *Proceedings of 5th International Conference & Exhibition on Multichip Modules*, pp. 15–21, 1996.
160. J. G. Aday et al., "A Comparative Analysis of High Density PWB Technologies," *Proceedings of 5th International Conference & Exhibition on Multichip Modules*, pp. 239–244, 1996.
161. A technical paper by Merix Corporation, "DYCO-strate® Technology," *CircuiTree*, pp. 44–54, June 1996.
162. K. Yamanaka et al., "High Performance Ball Grid Array Utilizing Flip Chip Bonding on Buildup Printed Circuit Board," *ECTC*, pp. 369–375, May 1997.
163. C. Lassen, "Microvias Where Silicon and Printed Circuit Technology Meet," *Future Circuits International*, Issue 4, pp. 25–28.
164. Y. Nakata et al., "A Wafer-Level Burn-in Technology Demonstration," *Proceedings of the 5th KGD Industry Workshop*, pp. 233–244, Sept. 1998.
165. R. Ghaffarian, "A Review of Chip Scale Package Assembly Reliability," *The 2nd International Conference on Chip Scale Packaging*, Feb. 1997.
166. E. Simeus et al., "CSP Consortia Activities: Program Objectives and Status," *Proceedings of the SMI Conference*, pp. 203–215, Sept. 1998.
167. High-density Packaging Users Group (HDPUG), Universal Instruments [140].
168. K. Boustedt et al., "The Chip Scale Packaging Task Force—Users and Manufacturers Working Together," *The 2nd International Conference on Chip Scale Packaging*, Feb. 1997.
169. *Nikkei Microdevices*, pp. 48–49, Apr. 1997.
170. C. L. Laassen and M. V. Christensen, "The Via Squeeze," *IEEE Spectrum*, pp. 36–41, Oct. 1999.
171. R. D. Schueller et al., "New Chip Scale Package with CTE Matching to the Board," *Proceedings of IEEE International Electronics Manufacturing Technology Symposium*, pp. 205–215, Oct. 1997.
172. C. Koehler et al., "A User-Focused Chip Scale Packaging Solution," *The 2nd International Conference on Chip Scale Packaging*, Feb. 1997.
173. T. Chung et al., "Wafer Level Packaging Technology," *Proceedings of the SEMICON West*, Session 3, pp. A1–A5, July 1999.
174. P. Elenius et al., "The Ultra CSP Wafer Scale Package," *Proceedings of the HDI Conference*, Mesa, AZ, pp. 541–547, Sept. 1998.
175. K. Nimmo, "Worldwide Environmental Issues in Electronics and the Transition to Lead Free," *Proceedings of IPCWORKS'99*, Minneapolis, MN, S-01-2, ITRI, Oct. 1999.
176. M. Watanabe and K. Ano, "Solder Joint Study of CSP for Use During the Transition Period To Lead Free Solders," *Proceedings of the Chip Scale Packaging Symposium*, San Jose, CA, pp. 12–19, Sept. 12–16, 1999.
177. P. Elenius and S. Yeh, "Lead Free Solder for Flip-Chip and CSP Applications," *Proceedings of IPC Summit on Lead-Free Assemblies*, Minneapolis, MN, Oct. 1999.
178. T. Chung et al., "Area Array Packaging

179

Technologies for High-Performance Computer Workstations and Multiprocessors," *ECTC Proceedings*, pp. 902–910, May 1996.

179. A. Babiarz, "Die Encapsulation and Flip Chip Underfilling Processes for Area Array Packaging of Advanced Integrated Circuits," *SMTA Proceedings*, pp. 125–137, Apr. 1997.

180. E. A. Logan et al., "Advanced Packaging of Intergrated Passive Device for RF Applications," http://www.intarsiacorp.com/chip_scale_frame.htm.

181. S. Wijeyeskera et al., "Development of Wafer Level Packaging for Integrated Passive Devices," *1999 International Conference on High Density Packaging and MCMs*, pp. 450–454.