DECLARATION OF
R. JACOB BAKER, Ph.D., P.E.
IN SUPPORT OF PETITION FOR *INTER PARTES*
REVIEW OF U.S. PATENT No. RE45,486

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I. Introduction

1. My name is R. Jacob Baker Ph.D., P.E. I am a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas. I have prepared this report as an expert witness on behalf of SanDisk LLC; Western Digital Corporation; and Western Digital Technologies, Inc. (collectively, "SanDisk"). In this report I give my opinions as to whether claims 6, 8-11, 22, 23, and 25-27 of U.S. Patent No. RE45,486 (the "'486 Patent") (Ex. 1001) are valid. I provide technical bases for these opinions as appropriate.

2. This report contains statements of my opinions formed to date and the bases and reasons for those opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses.

3. For my efforts in connection with the preparation of this declaration, I have been compensated at my standard rate for this type of consulting activity. My compensation is in no way contingent on the results of these or any other proceedings related to the '486 Patent.

4. I have summarized in this section my educational background, career history, publications, and other relevant qualifications. My full curriculum vitae is attached as Appendix A to this report.

A. Educational Background

5. I received a BS degree and a MS degree in electrical engineering from the University of Nevada, Las Vegas in 1986 and 1988 respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

B. Career History

6. I am a licensed Professional Engineer and have more than 30 years of experience, including extensive experience in circuit design and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips and CMOS Image Sensors (CISs) at Micron in Boise, Idaho. I also spent considerable time working on the development of Flash memory while at Micron. My efforts resulted in more than a dozen Flash memory related patents. One of my projects at Micron included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) Flash memory using signal processing for a 35 nm technology node. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that Micron DRAM products could transition to the DDR memory

command standard for addressing and controlling accesses to DRAM. I also provided technical assistance with Micron's acquisition of Photobit during 2001 and 2002. This assistance included help transitioning the manufacture of CIS products into Micron's DRAM process technology.

7. From 1985 to 1993 I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground weapon tests at the Nevada test site. During this time I designed over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/ transmitters, PLLs, frame- and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics.

8. I have been teaching electrical engineering since 1991. From 1991-1992, I was an adjunct faculty member in the electrical engineering department of the University of Nevada, Las Vegas.

9. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as an Associate Professor of Electrical Engineering.

10. In 2000, I joined a new electrical and computer engineering program at Boise State University where I served as department chair from 2004 to

2007. At BSU I helped establish graduate programs in electrical and computer engineering including, in 2006, the university's second Ph.D. degree.

11. In 2012, I re-joined the faculty at UNLV where I am currently a Professor of Electrical and Computer Engineering. Over the course of my career as a professor, I have advised over 75 graduate students.

12. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007 I received the Frederick Emmons Terman Award (the "Father of Silicon Valley") Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011 I received the IEEE Circuits and Systems Education Award. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award the four years I have been at UNLV.

13. I have more than 30 years of experience doing research and development in the area of electrical instrumentation in a multitude of areas including diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design,

CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits, circuit design for the use and storage of renewable energy, and power electronics.

14. I have also performed technical analysis and expert witness consulting for over 70 companies and laboratories. I have worked as a consultant at other companies designing memory chips and modules, including Sun, Oracle, and Contour Semiconductor. I have worked at other companies designing CISs, including Aerius Photonics, Lockheed-Martin, and OmniVision.

15. I have given more than 50 invited talks at conferences, companies, and Universities in the areas of integrated circuit design including: AMD, Arizona State University, Beijing Jiaotong University, Carleton University, Carnegie Mellon University, Columbia University, Dublin City University (Ireland), École Polytechnique de Montréal, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey, ITESM (Mexico), Iowa State University, Laval University, Lehigh University, Princeton University, Temple University, University of Alabama, University of Arkansas, University of Buenos Aires (Argentina), University of Illinois, Urbana-Champaign, Utah State University, University of Nevada, Las Vegas, University of Houston, University of Idaho,

University of Nevada, Reno, University of Macau, University of Toronto, University of Utah, Yonsei University (Seoul, Korea), University of Maryland, IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), the Franklin Institute, Georgia Tech, National Semiconductor, AMI semiconductor, Micron Technology, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Tower (Israel), Foveon, ICySSS keynote, and Xilinx.

C. Publications and Patents

16. I have authored many books and papers on circuit design. My published books include *CMOS Circuit Design, Layout, and Simulation* (Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Third Edition," *Wiley-IEEE*, ISBN: 978-0470881323 (2010)) and *CMOS Mixed-Signal Circuit Design* (Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, ISBN: 978-0470290262 (2nd ed., 2009) and ISBN: 978-0471227540 (1st ed., 2002)). I have also co-authored *DRAM Circuit Design: Fundamental and High-Speed Topics* (Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, ISBN: 978-0-470-18475-2), *DRAM Circuit Design: A Tutorial* (Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, ISBN: 0-7803-6014-1), and *CMOS Circuit Design,*

Layout and Simulation (Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, ISBN: 978-0780334168). I have also contributed as an editor and co-author on several other books on CMOS circuit design and VLSI.

17. I am the author and co-author of more than 100 papers and presentations in the areas of solid-state circuit design and packages. In 2000, I received the Best Paper Award from the IEEE Power Electronics Society.

18. I am a named inventor on 144 U.S. patents in integrated circuit design including flash memory, DRAM, and CMOS image sensors.

D. Other Relevant Qualifications

19. I currently serve, or have served, on: the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as a Distinguished Lecturer for the SSCS (2012-2015); and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-present) for the *IEEE Solid-State Circuits Magazine*. These meetings, groups, and publications are intended to allow researchers to share and coordinate

research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field were doing.

20. In addition to the above, I am an IEEE Fellow for contributions to memory circuit design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

E. Materials and Other Information Considered

21. I have considered information from various sources in forming my opinions, in addition to making use of my general knowledge of the relevant field, based upon my educational and work experience as set forth above. A list of exhibits I have reviewed is included herein as Appendix B.

II. Understanding of the Law

22. I have applied the following legal principles provided to me by counsel in arriving at the opinions set forth in this report.

A. Legal Standard for Prior Art

23. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim.

24. I understand that a U.S. or foreign patent qualifies as prior art to the claims of an asserted patent if the date of issuance of the patent is prior to the invention claimed in the asserted patent. I further understand that a printed publication, such as a book or an article published in a magazine or trade

publication, qualifies as prior art to the claims of an asserted patent if the date of publication is prior to the invention claimed in the asserted patent.

25. I understand that a U.S. or foreign patent qualifies as prior art to the claims of an asserted patent if the date of issuance of the patent is more than one year before the filing date of the asserted patent or the filing date to which the claims of the asserted patent are entitled to claim priority, whichever is earlier. I further understand that a printed publication, such as a book or an article published in a magazine or trade publication, constitutes prior art to an asserted patent if the publication occurred more than one year before the filing date of the asserted patent or the filing date to which the claims of the asserted patent are entitled to claim priority, whichever is earlier.

26. I understand that a U.S. patent qualifies as prior art to the asserted patent if the U.S. patent was granted on a patent application filed in the United States before the invention of the asserted patent. I understand that a U.S. patent application publication qualifies as prior art to the asserted patent if the publication was from a patent application filed in the United States before the invention of the asserted patent.

27. I understand that to qualify as prior art to the claims of an asserted patent, a reference must contain an enabling disclosure that allows one of

ordinary skill to make or use the claimed subject matter of the asserted patent without undue experimentation.

28. I understand that documents and materials that qualify as prior art can be used to invalidate a patent claim as anticipated or as obvious.

B. Legal Standard for Anticipation

29. I understand that once a claim of a patent has been properly construed, the second step in determining anticipation of that patent claim requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

30. I understand that a prior art reference "anticipates" an asserted claim, and thus renders the claim invalid, if that prior art reference discloses all the elements of the claim as arranged in the claim, either explicitly or inherently (*i.e.*, all elements are necessarily present or implied).

31. I understand that an asserted claim is anticipated if the claimed subject matter was known or used in the United States before the patent's inventor(s) invented the claimed subject matter.

32. I understand that a patent claim is anticipated if before the patent's inventor(s) invention thereof, the claimed subject matter was made in this country by another inventor who had not abandoned, suppressed, or concealed it.

33. I have written this report with the understanding that in an *inter partes* review anticipation must be shown by a preponderance of the evidence.

C. Legal Standard for Obviousness

34. I have been instructed by counsel on the law regarding obviousness, and understand that even if a patent claim is not anticipated, it is still invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the pertinent art.

35. I understand that a person of ordinary skill in the art provides a reference point from which the prior art and claimed invention should be viewed. This reference point prevents a person of ordinary skill from using one's insight or hindsight in deciding whether a claim is obvious.

36. I also understand that an obviousness determination includes the consideration of various factors such as (1) the scope and content of the prior art, (2) the differences between the prior art and the asserted claim, (3) the level of ordinary skill in the pertinent art, and (4) the existence of secondary considerations such as commercial success, long-felt but unresolved needs, failure of others, etc.

37. I am informed that secondary indicia of non-obviousness may include (1) a long felt but unmet need in the prior art that was satisfied by the invention of the patent; (2) commercial success or lack of commercial success of

processes covered by the patent; (3) unexpected results achieved by the invention; (4) praise of the invention by others skilled in the art; (5) taking of licenses under the patent by others; and (6) deliberate copying of the invention. I also understand that there must be a relationship between any such secondary indicia and the invention. I further understand that contemporaneous and independent invention by others is a secondary consideration supporting an obviousness determination.

38. I understand that an obviousness evaluation can be based on a combination of multiple prior art references. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the nexus linking two or more prior art references is simple common sense. I further understand that obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references may be supplied by the direction of the marketplace.

39. I understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

40. I also understand that practical and common sense considerations should guide a proper obviousness analysis, because familiar items

may have obvious uses beyond their primary purposes. I further understand that a person of ordinary skill in the art looking to overcome a problem will often be able to fit the teachings of multiple publications together like pieces of a puzzle, although the prior art need not be like two puzzle pieces that must fit perfectly together. I understand that obviousness analysis therefore takes into account the inferences and creative steps that a person of ordinary skill in the art would employ under the circumstances.

41. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

42. I understand that the combination of familiar elements according to known methods may be proven obvious when it does no more than yield predictable results. For example, when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious. In addition, when a work is available in one field of endeavor, design

incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, obviousness likely bars its patentability.

43. It is further my understanding that a proper obviousness analysis focuses on what was known or obvious to a person of ordinary skill in the art, not just the patentee. Accordingly, I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

44. I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in the reference can be supplied by the common sense of one of skill in the art.

45. I understand that a person of ordinary skill could have combined two pieces of prior art or substituted one prior art element for another if the substitution can be made with predictable results, even if the swapped-in element is different from the swapped-out element. In other words, the prior art need not be like two puzzle pieces that must fit together perfectly. The relevant question is whether prior art techniques are interoperable with respect to one another, such that that a person of skill would view them as a design choice, or

whether a person of skill could apply prior art techniques into a new combined system.

46. It is my understanding that prior art teachings are properly combined where a person of ordinary skill in the art having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

47. I have been informed and understand that the obviousness analysis requires a comparison of the properly construed claim language to the prior art on a limitation-by-limitation basis.

48. I have written this report with the understanding that in an *inter partes* review obviousness must be shown by a preponderance of the evidence.

D. Legal Standard for Claim Construction

49. I have been instructed by counsel on the law regarding claim construction and patent claims, and understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend

from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

50. It is my understanding that in proceedings before the USPTO the claims of an unexpired patent are to be given their broadest reasonable interpretation in light of the specification from the perspective of one of skill in the art. It is my further understanding that claim terms of an expired patent are given the meaning the term would have to a person of ordinary skill in the art at the time of the invention, in view of the specification and file history. I understand that the standard used for expired patents is similar to that used in district court litigation, and that this standard is sometimes referred to as the *Phillips* standard.

51. It is my understanding that the broadest reasonable interpretation of a claim term may be the same as or broader than the construction of a term under the *Phillips* standard, but it cannot be narrower.

52. In comparing the claims of the ’486 patent to the prior art, I have carefully considered the ’486 patent and its file history in light of the understanding of a person of skill at the time of the alleged invention.

53. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood disputed claim

language to mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent (all considered "intrinsic" evidence), and "extrinsic" evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.

54. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent specification, and the prosecution history.

55. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

56. I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the patent specification, and the prosecution history are of paramount importance. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

57. I understand that the claims of a patent define the scope of the rights conferred by the patent. The claims particularly point out and distinctly

claim the subject matter which the patentee regards as his invention. Because the patentee is required to define precisely what he claims his invention to be, it is improper to construe claims in a manner different from the plain import of the terms used consistent with the specification. Accordingly, a claim construction analysis must begin and remain centered on the claim language itself. Additionally, the context in which a term is used in the asserted claim can be highly instructive. Likewise, other claims of the patent in question, both asserted and unasserted, can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims. Differences among claims can also be a useful guide in understanding the meaning of particular claim terms.

58. I understand that the claims of a patent define the purported invention. I understand that the purpose of claim construction is to understand how one skilled in the art would have understood the claim terms at the time of the purported invention.

59. I understand that a person of ordinary skill in the art is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. For this reason, the words of the claim must be interpreted in view of

the entire specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim as set forth in the patent itself.

60. I understand that it is improper to place too much emphasis on the ordinary meaning of the claim term without adequate grounding of that term within the context of the specification of the asserted patent. Hence, claim terms should not be broadly construed to encompass subject matter that, although technically within the broadest reading of the term, is not supported when the claims are read in light of the invention described in the specification. Put another way, claim terms are given their broadest reasonable interpretation that is consistent with the specification and the prosecution history. Art incorporated by reference or otherwise cited during the prosecution history is also highly relevant in ascertaining the breadth of claim terms.

61. I understand that the role of the specification is to describe and enable the invention. In turn, the claims cannot be of broader scope than the invention that is set forth in the specification. Care must be taken lest word-by-word definition, removed from the context of the patent, leads to an overall result that departs significantly from the patented invention.

62. I understand that claim terms must be construed in a manner consistent with the context of the intrinsic record. In addition to consulting the specification, one should also consider the patent's prosecution history, if available. The prosecution file history provides evidence of how both the Patent Office and the inventors understood the terms of the patent, particularly in light of what was known in the prior art. Further, where the specification describes a claim term broadly, arguments and amendments made during prosecution may require a more narrow interpretation.

63. I understand that while intrinsic evidence is of primary importance, extrinsic evidence, e.g., all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may help one better understand the underlying technology and the way in which one of skill in the art might use the claim terms. Extrinsic evidence should not be considered, however, divorced from the context of the intrinsic evidence. Evidence beyond the patent specification, prosecution history, and other claims in the patent should not be relied upon unless the claim language is ambiguous in light of these intrinsic sources. Furthermore, while extrinsic evidence can shed useful light on the relevant art, it is less significant than the intrinsic record in determining the legally operative meaning of claim language.

64. I understand that in general, a term or phrase found in the introductory words of the claim, the preamble of the claim, should be construed as a limitation if it recites essential structure or steps, or is necessary to give life, meaning, and vitality to the claim. Conversely, a preamble term or phrase is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. In making this distinction, one should review the entire patent to gain an understanding of what the inventors claim they actually invented and intended to encompass by the claims.

65. I understand that language in the preamble limits claim scope (i) if dependence on a preamble phrase for antecedent basis indicates a reliance on both the preamble and claim body to define the claimed invention; (ii) if reference to the preamble is necessary to understand limitations or terms in the claim body; or (iii) if the preamble recites additional structure or steps that the specification identifies as important.

66. I understand that 35 U.S.C. § 112 ¶ 6 created an exception to the general rule of claim construction. In particular, I understand that a "means plus function" limitation should be interpreted to cover only the corresponding structure described in the specification, and equivalents thereof. I also understand that a limitation will be presumed to be a means plus function limitation if (a) the

claim limitation uses the phrase "means for"; (b) the "means for" is modified by functional language; and (c) the phrase "means for" is not modified by sufficient structure for achieving the specified function. I further understand that formulations other than "means for" may also invoke 112 ¶ 6, such as when a claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function.

67. I understand that a structure will be considered structurally equivalent to the corresponding structure identified in the specification only if the difference between them are insubstantial. For example, a structure may be deemed to be a structural equivalent to the corresponding structure where the structure performs the same function in substantially the same way to achieve substantially the same result. I further understand that a structural equivalent must have been available at the time of the issuance of the claim.

E. Legal Standard for Priority Date

68. I understand that the "critical date" for a patent claim is one year prior to the patent's filing date or one year prior to the date to which the patent claim is entitled to claim priority, whichever is earlier. It is my understanding that the critical date is significant because patents, systems, or documents that are public prior to the critical date, if they disclose each and every limitation of a

claim, will invalidate that claim regardless of whether the inventors invented the claimed subject matter.

69. I understand that the "priority date" of a patent is the date on which it is filed, or the date on which an earlier-filed patent application is filed if the patentee claims the benefit of priority to that earlier-filed patent application. I further understand that the priority date is significant because patents, systems, or documents that are public less than one year prior to the priority date may invalidate the claims. My understanding is that, for such prior art references, a patentee may attempt to show that the claimed invention was conceived prior to the publication date of the prior art reference.

70. I understand that a patent may be valid over prior art that was published or was publicly available before the priority date but after the critical date. To do so, it is my understanding that patentee must prove with corroborating evidence that the named inventors conceived of the claimed invention before the prior art, and were diligent in reducing the claimed inventions to practice.

III. Level of Skill of One of Ordinary Skill in the Art

71. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '486 patent at the time of the claimed inventions (which I take to be February 2003), I considered several things, including various prior art techniques for managing write protection of memory devices, the type of

problems that such techniques gave rise to, and the rapidity with which innovations were made. I also considered the sophistication of the technologies involved, and the educational background and experience of those actively working in the field. I also considered the level of education that would be necessary to understand the '486 Patent. Finally, I placed myself back in the relevant period of time, and considered the academics, engineers, and students that I had worked with in the field of electrical and electronic engineering. I came to the conclusion that the characteristics of a person of ordinary skill in the field of art of the '486 patent would be a person with a bachelor's degree in electrical engineering or a closely related field, and two to three years of experience in the field of memory system design. A person with less education but more relevant practical experience, or with less experience but more education, may also meet this standard.

IV. Technology Background

72. In what follows, I will provide an overview of technologies relevant to the accused systems.

73. The '486 Patent is directed to systems and methods for addressing the memory locations of a card.

A. Overview of Memory Devices and Addressing

74. Memory cards, such as PC cards, compact flash ("CF") cards, secure digital ("SD") cards, or multimedia cards ("MMC"), are electronic data

storage devices used in various portable electronic devices such as PDAs, cameras, and smart phones. Ex. 1005 at 1:19-22. Data is stored on a memory device by recording the data in memory cells, such as flash or EEPROM. *Id*. at 1:30-35.

B. Specification and Control of MMCs

75. Unveiled in 1997, the MMC standard is a memory card standard used for solid-state storage based on a surface contact low pin-count serial interface using a single memory stack substrate assembly. Ex. 1010. MMCs can be implemented as mass storage cards with one or more memory technologies such as ROM, OTP, MTP, or Flash.

76. A MMC system comprises a group of registers (*e.g.*, OCR, CID, CSD, RCA, DSR) for storing a variety of status and internal information. Ex. 1005 at 9:45-49. The registers are used for providing information to the host computing system and for determining the communication protocol between the host and the MMC. *Id*. at 49-51. The host can access the registers by issuing a specific set of commands. Ex. 1005 at 9:51-55.

77. The CSD (card specific data) register is responsible for providing information to the host computing system on how to access the card content. *Id*. at 10:24-26. Specifically, the CSD register stores values defining the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used, etc. *Id*. at 10:24-29.

78. Entries of the CSD register may be denoted as R=readable, W=writable once, or E=erasable (multiple writable). *Id*. at 10:29-31.

79. A MMC and a host device of the MMC are connected by a CMD bus line for communication of commands and responses and a DAT bus line for transmission of data. Ex. 1005 at 7:57-65.

80. A MMC is controlled by commands, which are related to operations such as data read, data write, changing card status, or obtaining card information. *Id*. at FIGs. 38-44. Many commands use an address as a command argument to identify a location on the memory card to be accessed. *Id*. at 9:51-55.

C. Addressing Methods and Capacity

81. Addressing enables the access of data. Over time, the need to expand the capacity of memory systems required the incorporation of expanded methods of addressing into existing methods of addressing. As computer memory and capability expanded, there arose a need to increase addressing in a number of contexts– memory cards (PCMCIA), flash memory, MMC, disk drives, etc..

82. Also common was the need to access addressing at different levels of granularity. For example, computers have used virtual memory for decades. A common way of doing this is to select the page size 0 that is the smallest unit that gets read and written in response to an address. The desirability

of increasing capacity, and established technique for doing so, was well known at the time the '486 patent was filed.

83. For example, U.S. Patent 6,260,101 to Hanzen described this issue. Ex. 1011. Hanzen describes how early x86 processors used 20-bit addresses that comprised a 16-bit "segment" portion of the address, and a 16-bit "offset portion, and how newer x86 processors maintain the same address generation for reasons of backward compatibility. Ex. 1011 at 2:5-24. Hanzen further describes a system that uses an "auxiliary address generator (AAG)" to combine ordinary address signals (20-bits) with "auxiliary" address signals that make up the most significant bits, so that the memory can be expanded into a set of banks. Ex. 1011 at 2:26-34; 7:1-11; 19:19-20:9; Fig. 13.

84. Computer devices often organized memory in a hierarchy with relatively expensive high speed devices (typically close to the processor) and relatively inexpensive lower speed but higher capacity speed (further from the processor). To manage these hierarchal arrangements of different data stores, computer systems have employed addressing methods including virtual addressing and paging, cache management, and a variety of different hardware and software mechanisms to ensure the consistency of data stored sometimes in multiple locations within these memory hierarchies. *See*, Ex. 1012.

85. One solution was the use of higher and lower order bits for addressing. A person having training in computer system and design would know that addressing based on a subset of bits and adjusting the size of the chunk of data that being is accessed is a standard design technique. Ex. 1012, 408-416. In the case of caches for example, a small, fast memory - the cache - is used to store heavily used memory words for access by the CPU in order to improve the speed at which the computer functions. Ex. 1012 at 65. The cache is divided into fixed-size blocks, referred to as cache lines. *Id*. at 67. A cache manages memory addressing using a subset of address bits (cache tag) to determine whether a particular cache line is present in the cache or not. *Id*. at 67. The lowest order bits, or block index bits, can be used by a system to point to an individual piece of data within a cache line, but with regard to accesses to main memory, the cache ignores these bits because accesses are performed only at the level of granularity of an entire block or cache line. *Id*. at 267-268. For example, in the case of a 32-byte cache line size, the lowest order bits 0-4 are not part of the addressing method since the cache only accesses chunks of data that are 32 bytes long and aligned by a 32-byte block size. *Id*.

86. A person having training in computer system and design would know that addressing based on a subset of bits and adjusting the size of the chunk of data that being accessed is the most standard design technique that is

implemented by all computers that use caches for the management of the cache. The notion of essentially a course memory storage system in which it is possible to access things in "chunks" of that size is a standard design technique used in almost every computer design. Ex. 1012 at 408-416.

87. Further, a person having skill in the art would recognize that there are multiple design criteria for instruction formats in computer design. *Id*. at 322. One such criterion concerns the number of bits in an address field. *Id*. at 324. For example, one could choose to make the 8-bit byte as the basic unit of memory, or instead one could choose to make the 32-bit word the basic unit of memory. Both selections have benefits and drawbacks. One of skill in the art would recognize that "in order to gain a finer memory resolution, one must pay the price of longer addresses and thus longer instructions." *Id*. 324.

88. In another example, U.S. Patent 6,253,300 to Lawrence et al. describes changing cluster size of a file system on the fly to change the amount of data accessed with a command. Ex. 1013 at Abstract. The method described in Lawrence allows disk imaging to me more flexible and more efficient by locating and organizing file system structures in memory for easier access. Ex. 1013 at 7:40-45. Further, changing the cluster size can enable defragmenting to permit more efficient use of available memory space. Ex. 1013 at 10:56-60.

89. Computer systems typically manage main system memory using the same concept. Memory is subdivided into chunks of consecutive addresses known as pages. Ex. 1012 at 406. Memory addresses are often broken into a virtual page number and a page offset. *Id.* at 407. Since the physical memory is often much smaller than the total address space, a computer will swap pages of data into and out of physical memory and maintain a table (known as the page table) by which the operating system can tell which pages of data are actually resident in the machine's memory. *Id*. at 406-407. In accessing data, the highest order bits of a virtual address are known as the virtual page number and the system translates virtual page numbers into physical pages. *Id*. at 407. The choice of the page size is an engineering trade off that balances the efficiency of memory utilization (small page size) against the size of the data structure needed for addressing pages. Again, there are trade-offs between granularity with the smallest chunk of data a system accesses and the number of bits needed to access it are routinely made in the design of data storage systems.

V. The '486 Patent

A. Summary of the '486 Patent

90. I have reviewed the '486 Patent, which is entitled "Method For Addressing A Memory Card, A System Using A Memory Card, And A Memory Card." I understand that the application that later issued as the '486 Patent was

filed on May 24, 2013. I also understand that the '486 Patent claims foreign priority to European Patent Appl. No. 20030191, which was filed February 7, 2003.

91. The '486 Patent is directed to a method, system, and memory card for addressing the memory locations of a memory card.

92. According to the background section of the '486 Patent, memory card can be connected to different electronic devices for storing data and for using the stored data. Ex. 1001 at 1:58-59. Such "[m]emory cards can comprise a semiconductor memory, where there are several memory locations that can be addressed." *Id*. at 1:60-62. Each memory location typically comprises a specific number of bits, such as 8 bits (a byte), 16 bits (a word), etc.. *Id*. at 1:62-65. The background of the '486 Patent discloses that memory cards have been developed such that data can be transferred between the memory card and an external device block by block, i.e. as assemblies of memory locations. *Id*. at 2:1-4.

93. According to the background section of the '486 Patent, "a problem [has arisen] of, e.g. how the memory space of [an] entire memory card can be handled." *Id*. at 2:28-30. The background section contemplates that "in some memory card standard an upper limit has been set for the number of memory locations included in a memory card." *Id*. at 2:19-21. The background section further contemplates that developments in semiconductor memories and other

memory techniques have "made it possible to substantially reduce the area requires for storing one bit," such that "the amount of memory that can be fitted into a memory card is nowadays already larger than the upper limit determined by many standards." *Id*. at 2:21-26.

94. The background section of the '486 frequently refers to the MultimediaCard ("MMC") specification in force at the time, stating: "in order to address the memory locations of a memory card according to the specifications of [a] Multimedia Card, there are 32 bits that can be used, with which a maximum of 4 gigabytes of memory space can be addressed." *Id*. at 2:31-34. The background section further states that "[t]he maximum memory capacity of the memory card according to the MultiMedia Card specifications is especially limited by the fact that data on the memory capacity of the memory card is coded in the memory card." *Id*. at 2:38-42.

95. The memory capacity of a memory card according to the MMC specification was calculated by multiplying the number of blocks with the length of the block. *Id*. at 42-44. The MMC specification provides that the number of blocks (BLOCKNR) can be determined by reading the parameters C_SIZE and C_SIZE_MULT stored in the memory, as well as by performing the calculation: $BLOCKNR=(C\_SIZE+1)*^{2C\_SIZE\_MULT+2}$. *Id*. at 2:43-49. The MMC specification further provides that the length of the block (BLOCK_LEN) is determined by

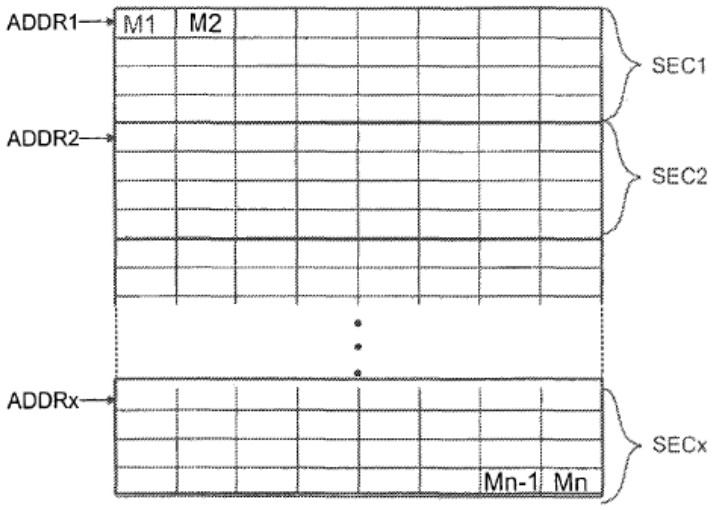
means of the parameter READ_BL_LEN in the following way: $BLOCK\_LEN=2^{READ\_BL\_LEN}$. *Id*. at 2:50-54. According to the background section of the '486 Patent, "12 bits are reserved for the parameter C_SIZE, in which case the maximum value is 4095." *Id*. at 2:55-58. Further, "[t]hree bits are reserved for the parameter C_SIZE_MULT, while the maximum value is 7" and "[f]our bits are reserved for the parameter READ_BL_LEN, and therefore the maximum value is 16." *Id*. at 2:58-60. According to the background of the '486 Patent, "from the 4 bit values of the parameter READ_BL_LEN, only the values 0 to 11 are in use." *Id*. at 2:60-62. The '486 Patent asserted that on the basis of these parameters and values, the maximum capacity of a memory card according to the MMC specification is 4 gigabytes. *Id*. at 2:62-67.

96. The '486 Patent purports to disclose a method, system, and memory card "for addressing the memory locations of a memory card. *Id*. at Abstract. In particular, the '486 Patent discloses a method in which "two or more memory locations are addressed with one address, and/or the number of bits that can be used in an address is increased." *Id*. at Abstract.

97. The '486 Patent purports that "by applying the invention, it is possible to create memory card, where the memory capacity is significantly larger than in memory card according to prior art." *Id*. 3:31-34. The '486 Patent also

alleges that "total power consumption can be reduced in the device according to the invention." *Id*. at 3:43-44.

98. In one embodiment, "the memory locations of the memory card are handled in a so called sector-by-sector manner, in which case with one address ADDR1 it is possible to address to the data of one sector SEC2, with the next address ADDR2 to the data of the next sector SEC2, etc." *Id*. at 5:41-46. The '486 Patent purports that "with one reading address the data of the memory locations M1, M2, ..., Mn of one sector is read." *Id*. at 5:46-48. Figure 2 of the '486 patent illustrates this embodiment:



99. In this embodiment, "[d]ata on that the memory card functions in a sector-based manner is stored in the memory card." *Id*. at 5:51-52. The '486 patent asserts that "[t]his addressing data is stored preferably in one bit, as which is used, for example, a bit not in use by the CSD register." *Id*. at 5:52-54.

100. The size of the sector may vary in different situations. *Id*. at 5:50-51. Further, "the size of the sector is not necessarily the same as the size of the [memory] block, but it can be smaller or larger than the size of the [memory] block. *Id*. at 5:59-61. The "size of the sector of the memory card is stored in the registers of the memory as well." *Id*. at 5:66-67. According to the '486 Patent, this enables the MMC memory card "to use the register READ_BL_LEN indicating the [memory] block size" to calculate the capacity of the memory card. *Id*. at 6:1-4.

101. In this embodiment, the significance of the parameters of the formula used to calculate memory card capacity for a memory card according to the MMC specification changes. *Id*. at 6:14-20. Particularly, "the parameter C_SIZE has been change[d] so that it signifies kilobytes instead of bytes." *Id*. at 6:21-23. Accordingly, the maximum memory capacity is 4 terabytes. *Id*. at 6:24-33.

102. In another embodiment, the increase of the memory capacity of the memory card is implemented by using additional values for the parameter READ_BL_LEN to increase BLOCK_LEN, upon which the memory card capacity can be calculated. *Id*. at 7:50-54. As discussed with reference to the prior art, the MMC specification uses values 0-11 for the parameter READ_BL_LEN. *Id*. at 2:61-62. The '486 Patent discloses using additional values 12-15 for the parameter

READ_BL_LEN, such that the maximum memory capacity is 64 gigabytes. *Id*. at 7:54-60.

103. In a third embodiment, "the number of address bits is increased" to increase the memory capacity of a memory card. *Id*. at 8:42-43. This embodiment is implemented "preferably by doubling the number of address bits from, for example, 32 bits to 64 bits." *Id*. at 8:43-44. In this embodiment, values 12-15 are taken into use in the parameter READ_BL_LEN as described above. *Id*. at 8:40-42. In this embodiment, the value of parameter READ_BL_LEN is used to calculate the maximum memory capacity and in determining the size of the memory blocks. *Id*. at 8:50-53.

104. In this third embodiment, "the increase in the number of address bits can be implemented by several means." *Id*. at 9:5-6. One option is that "a special command is specified, which indicates to the memory card that it is an expanded address." *Id*. at 9:7-8.

105. This "type of special command can be implemented in the present command register CSD or in the expanded command register EXT_CSD." *Id*. at 9:11-14. Another possibility is to use a switch-command, wherein "the parameter of the switch command [...] indicates which command is in question at a certain time." *Id*. at 9:14-17.

106. Finally, the '486 Patent alleges that memory cards according to the invention are downwards compatible, such that when a memory card according to the invention is connected to a device where the changes required for using the memory card according to the invention have not been implemented, the memory card still functions, from the point of view of the device, as a memory card according to the prior art. *Id*. at 9:20-27.

107. However, as I discuss below with respect to the prior art, the techniques disclosed in the '486 Patent were well known in the art.

B. '486 Patent Prosecution History

108. On February 7, 2003, the Applicant filed a Finnish Patent Application No. 200330191, which issued as Finnish patent 117489 on October 31, 2006.

109. On February 2, 2004, the Applicant filed U.S. Patent Application No. 10/770,852 ("the '852 Application). Ex. 1004 at 182-203. This application ultimately issued as U.S. Patent No. 7,257,669 to Marko Ahvenainen and Kimmo Mylly ("the '669 Patent) on August 14, 2007. Ex. 1003.

110. On October 6, 2006, the Examiner rejected pending claims 1-20 of the '852 Application under 35 U.S.C. § 103(a) as being obvious over Applicant's Admitted Prior Art (AAPA) in view of U.S. Patent No. 6,023,281 to Grigor et al. ("Grigor"). Ex. 1004 at 43-51. The Examiner also objected to the

clause "on the basis of which parameter the number of memory locations" of the specification at page 1, lines 15-17 and 33-34 as indefinite. *Id*. The Examiner objected to claims 1, 10, 13, and 15 because the clause "on the basis of which parameter the number of memory locations" was indefinite. *Id*. The Examiner also objected to the device of Claim 17 as lacking proper antecedent basis in the claim. *Id*.

111. On January 8, 2007, the Applicant filed an Amendment to amend claims of the '852 Application. Ex. 1004 at 30-41. The Applicant amended claims 1, 10, 13, and 15 to overcome Examiner's indefiniteness objection. *Id*. at 38. The Applicant also amended claim 17 to overcome the Examiner's objection due to lack of proper antecedent basis. *Id*. at 36; 38. The Applicant amended the specification at page 1, lines 15-17 and 33-34 to overcome Examiner's indefiniteness objection. *Id*. at 31. Further, Applicant added Claim 21, alleging that added Claim 21 "corresponds to Claim 10, but written in means plus function format." *Id*. at 37-38.

112. In Applicant's January 8, 2007 response, Applicant amended claims 1, 2, 10, 11, 13, 15, and 16 of the '852 Application in an effort to overcome the Examiner's obviousness rejection under 35 U.S.C. § 103(a). *Id*. at 38. Applicant argues that the amendment to Claim 1 incorporates "a part of the feature recited in original claim 2." *Id*. at 39. Applicant argued that, as amended, Claim 1

"is directed to an important part of the present invention as specifically described at page 8, lines 14-17 of the specification, wherein it is stated: Data on the memory card functions in a sector-based manner is stored in the memory card. This addressing data is stored preferably in one bit, as which is used, for example, a bit not used by the CSD register." *Id*. Applicant further argued that "[t]he addressing method may be byte addressing or sector addressing." *Id*. Applicant also argued that "[t]he invention is a usage of a sector address instead of a byte address and, more particularly, adapting to the type of addressing modes supported (for example, such as byte or sector addressing) as indicated by the memory device." *Id*.

113. In this same response, Applicant argued that the disclosure of "the MultimediaCard specification relied upon by the Office with respect to the AAPA as asserted with respect to claim 2 is data parameters on the memory capacity according to the MultimediaCard specifications." *Id*. at 39-40. Applicant argued that "[m]emory capacity and an addressing method used (such as byte addressing or sector addressing) are not the same nor are they equivalent to each other" and that "[t]he addressing method is not necessarily dependent on the memory capacity of the card." *Id*. at 40. Accordingly, Applicant alleged that "the AAPA does not disclose or suggest storing in a memory card an addressing data wherein that addressing data is indicative of an addressing method used as required

by claim 1." *Id*. With respect to Grigor, the Applicant argued that in Grigor, "the mapping [portions of a shared memory] is performed such that either of the processors' portions can be enlarged or reduced based on the memory that is located between the portions allocated to the processors." *Id*. Accordingly, according to Applicant, Grigor did not suggest "storing in a memory card an addressing data being indicative of an addressing method used." *Id*.

114. In the same response, the Applicant also amended Claim 2 of the '852 Application to read "The method of claim 1, comprising at least one of the following: addressing two or more memory locations with one address; increasing the number of bits that can be used in an address." *Id*. Applicant argued that this claim was "further distinguished over the cited art in view of the fact that data or parameters on memory capacity as set forth in the MultiMediaCard specification is not in any way related to the type of addressing used with respect to the memory card." *Id*.

115. On May 4, 2007, the Office mailed a Notice of Allowance which allowed claims 1-21 as amended in Applicant's Response to Office Action on January 8, 2007. *Id*. at 17-20.

116. On August 14, 2007, the '852 Application issued as the '669 Patent. *Id*. at 15.

117. On November 9, 2007, the Applicant filed a Request for Certificate of Correction of Patent for PTO Mistake under 37 C.F.R. 1.322(a). *Id*. at 11-14. The Request identified five errors in the specification of the '669 Patent. *Id*.

118. On February 15, 2008, the Office approved Applicant's Request for Certificate of Correction. *Id*. at 8.

119. The '486 Patent is a reissued patent of U.S. Patent 7,257,669.

120. The '486 Patent originated from reissue Application No. 13/902,258 ("the '258 Application") filed on May 24, 2013, which sought to cancel claims 2 and 7. Ex. 1002 at 299-306. Claims 2 and 7 previously claimed the system of Claim 1 and the memory card of claim 6, respectively, "comprising at least one of the following: addressing two or more memory locations with one address; increasing the number bits that can be used in an address." Ex. 1003 at 10:19-25; 10:62-67. The Preliminary Amendment also sought to add to claim 6 "wherein the addressing data indicates either a basic addressing method or an expanded addressing method, and wherein the expanded addressing method supports a higher memory capacity than the basic addressing method." Ex. 1002 at 299-306. The Preliminary Amendment amended claim 8 to claim "a memory card according to claim 6, comprising a bus connection block for connecting the memory card to a device and for transferring data between the device and the

memory card." *Id*. at 301. Finally, the Preliminary Amendment sought to add new claim 22 which claimed "the memory card of claim 6, wherein the card is configured to address one memory location when using the basic addressing method and two or more memory locations when using the expanded addressing method." *Id*. at 304.

121. On May 12, 2014, the Examiner issued a rejection of all of the claims of the reissue Application '258. The Examiner rejected each of claims 1, 3-6, 8-16, and 22 as being anticipated by U.S. Patent No. 6,901,457 to Toombs et al. ("Toombs '457"). *Id*. at 76-86. The Examiner rejected each of claims 17-21 under § 103(a) as unpatentable over Toombs '457 in view of Applicant Admitted Prior Art (AAPA). *Id*.

122. On August 11, 2014, the Examiner filed an Applicant-Initiated Interview Summary stating that the issue discussed was the Examiner's anticipation rejection of Application '258. *Id*. at 17-18. According to the Interview Summary, the "Applicant explained in further details the claimed invention." *Id*. at 17. The Interview Summary further states that "[b]ased on the discussion, it is clear that new claims are expected to be filed and claim 6, at least, is expected to be amended to mere clearly define the claimed invention." (typographical error in original). *Id*. Finally, the summary noted that "Applicant stated that the other independent claims would be further be reviewed in order to bring the independent

claims into the same line as the amendment that is to be carried to independent claim 6." *Id*.

123. On August 12, 2014, the Applicant filed an Amendment to amend claims 1, 4, 6, 12, 13 and 22 of the '258 Application. *Id*. at 51-69. Applicant also added new claims 23-31. *Id*. The Applicant argued that "the Examiner improperly equates a 'card address' in the RCE register with the claimed 'addressing data being indicative of at least one addressing method supported,' as recited in claims 1, 4, 6, 12, 13, 10 and 31." *Id*. at 65. The applicant pointed to the '669 Patent specification for a "non-limiting example" of two different addressing methods: an "expanded addressing method" and a "basic addressing method." *Id*. The Applicant argued that Examiner's reliance on Toombs '457 was improper because "merely using a 'card address' to identify a card to be used for host communication does not teach the claimed 'addressing data being indicative of at least one addressing method supported.'" *Id*. The Applicant further argued that "Toombs lack the disclosure of at least 'wherein the expanded addressing method enables the addressing of data in a larger number of memory locations than the basic addressing method,' as claimed." *Id*. In addition, the Applicant argued that features disclosed in new independent claims 30 and 31 distinguish over Toombs. *Id*. at 67. As to claims 17-21, the Applicant argued that the obviousness rejection was improper because the Examiner had not met the "high burden required for the

Examiner to be able to allege AAPA." *Id*. 67-68. The Applicant also argued that "even if there is AAPA, it is not used by the Examiner" to disclose a distinguishing feature of claim 13, from which claims 17-21 depend. *Id*.

124. On March 2, 2015, the Examiner issued a Notice of Allowance for claims 1, 3-6, and 8-31 of the '258 Application. *Id*. at 10-16.

125. The '258 Application issued as RE45,486 ("the '486 Patent") on April 21, 2015. *Id*. at 1.

VI. The Challenged Claims

126. The '486 Patent has twenty nine claims. I have considered invalidity with respect to claims 6, 8-11, 22, 23, 26, and 27. The challenged claims are set forth below:

i. Claim 6

A memory card comprising:

several memory locations for storing data, and in which memory card is stored at least one parameter , the memory card configured so that the number of memory locations of the memory card can be calculated on the basis of said at least one parameter,

the memory card configured so that a specific number of bits is reserved for said at least one parameter, and

the memory card further configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported,

wherein the addressing data indicates either a basic addressing method or an expanded addressing method, and

wherein the expanded addressing method enables the addressing of data in a larger number of memory locations than the basic addressing method.

ii. Claim 8

The memory card according to claim 6, comprising a bus connection block for connecting the memory card device to a device and for transferring data between the device and the memory card.

iii. Claim 9

The memory card according to claim 6, wherein data is arranged to be stored and read in the memory card block-by-block.

iv. Claim 10

The memory card according to claim 9, wherein the memory locations of one block are arranged to be addressed with one address.

v. Claim 11

The memory card according to claim 6, wherein the memory card is a memory card according to MultiMediaCard specifications.

vi. Claim 22

The memory card according to claim 6, wherein the basic addressing method supports addressing only one memory location with one address.

vii. Claim 23

The memory card according to claim 6, wherein the expanded addressing method supports a higher capacity than the basic addressing method.

viii. Claim 25

The memory card according to claim 6, wherein the memory card is configured so that, if the addressing data indicated that the memory card supports the expanded addressing method, the memory card uses the expanded addressing method in response to a successful reading of the addressing data that indicated support of the expanded addressing method.

ix.Claim 26

The memory card according to claim 6, further comprising a register for storing the addressing data.

x. Claim 27

The memory card according to claim 26, wherein the stored addressing data comprises one bit.

VII. Claim Construction

127. I have carefully considered the '486 Patent and its file history based on my experience and knowledge in the field, and I believe the following terms should have the following meanings from the perspective of one of ordinary skill in the art.

A. "addressing data"

128. Challenged claims 6, 8-11, 22, 23, and 25-27 all recite "addressing data." One of ordinary skill in the art would have recognized that the broadest reasonable interpretation of this phrase is "data indicative of an addressing method."

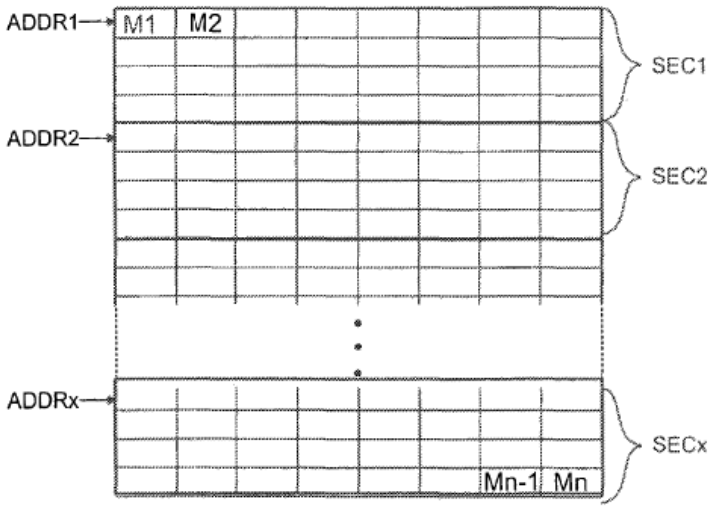
129. "[A]ddressing data" is not a term of art. The specification of the '486 Patent describes one embodiment in which an indication "that the memory card functions in a sector-based manner" is stored preferably in one bit and constitutes "addressing data." Ex. 1001 at 5:51-54; Ex. 1004 at 38-41. The specification of the '486 Patent further describes that the "value of the addressing data is stored to the memory card advantageously in the manufacturing phase of the memory card." Ex. 1001 at 5:57-59.

130. Based on the specification, one of ordinary skill in the art would have recognized that the broadest reasonable interpretation of "addressing data" is "data indicative of an addressing method."

B. "an addressing method"

131. Challenged claims 6, 8-11, 22, 23, and 25-27 all recite "an addressing method." One of ordinary skill in the art would have recognized that the broadest reasonable interpretation of this phrase is "a technique of accessing data by way of its location."

132. "[A]n addressing method" is not a term of art. The specification of the '486 Patent describes that "[i]t is an aim of the present invention to provide an improved addressing method for addressing memory locations of a memory card." Ex. 1001 at 3:3-4. The patent states: "FIG. 2 shows an addressing method according to an advantageous embodiment of the invention in a reduced manner." Ex. 1001 at 3:55-56. Figure 2 of the '486 Patent is shown below:



133. The specification describes three embodiments. Ex. 1001 at 1:41-46; 7:49-55; 8:37-49. During prosecution of the '669 Patent, the Applicant argued that "[t]he addressing method may be byte addressing or sector

addressing." Ex. 1004 at 39. The Applicant asserted that "[t]he invention is a usage of a sector address instead of a byte address and, more particularly, adapting to the type of addressing modes supported (for example, such as byte or sector addressing) as indicated by the memory device." *Id*. Further, the Applicant argued that "[m]emory capacity and an addressing method used (such as byte addressing or sector addressing) are not the same nor are they equivalent to each other." *Id*.

134. During prosecution of the '486 Patent, the Applicant argued that "[a]s a non-limiting example from the '669 patent specification, two different supported addressing methods may include an 'expanded addressing' method and a 'basic addressing' method." Ex. 1002 at 65(citing the '669 Patent at 9:39-58).

135. Accordingly, one of ordinary skill in the art would have recognized that the broadest reasonable interpretation of "an addressing method: is "a technique of accessing data by way of its location."

C. "addressing of data"

136. Challenged claims 6, 8-11, 22, 23, and 25-27 all recite "addressing of data." One of ordinary skill in the art would have recognized that the broadest reasonable interpretation of this phrase is "identifying a portion of memory for a data operation."

137. The specification does not describe the "addressing of data." Nor is this term defined in the prosecution history of the '669 Patent or the '486 Patent.

138. Based on the lack of description in specification, one of ordinary skill in the art would have recognized that the broadest reasonable interpretation of "addressing of data" is "identifying a portion of memory for a data operation."

D. "memory location"

139. Challenged claims 6, 8-11, 22, 23, and 25-27 all recite "memory location." One of ordinary skill in the art would have recognized that the broadest reasonable interpretation of this phrase is "a location in memory where data is stored."

140. The specification of the '486 Patent describes semiconductor memory, "where there are several memory locations that can be addressed." Ex. 1001 at 1:60-62. The specification further explains that a memory location is not limited to a particular size, stating: "[e]ach memory location typically comprises a specific number of bits, such as 8 bits (a byte), 16 bits (a word), 32 bits (a double-word), or even 64 bits." *Id*. at 1:62-65. Accordingly, "the amount of data that can be addressed with one piece of address data is the amount of bits in the memory location in question." *Id*. at 1:65-67.

141. Accordingly, one of ordinary skill in the art would have recognized that the broadest reasonable interpretation of "memory location" is "a location in memory where data is stored."

VIII. Analysis of the Prior Art

142. There are a number of patents and publications which constitute prior art to the '486 Patent. I have reviewed and considered the following prior art patent and printed publications, which I believe were all publicly available and/or filed with the United States Patent and Trademark Office prior to February 2, 2003, the claimed priority date. A description of these references follows.

- U.S. Patent Number 6,279,114 to Toombs et al. ("Toombs"), entitled "Voltage Negotiation in a Single Host Multiple Cards System," filed November 4, 1998, and issued August 21, 2001 (Ex. 1005)
- U.S. Patent Number 6,314,504 to Dent ("Dent"), entitled "Multi-Mode Memory Addressing Using Variable-Length," filed March 9, 1999, and issued November 6, 2001 (Ex. 1006)
- PC Card Standard, Volume 2 Electrical Specification ("PCMCIA"), publicly available online as of November 2001 (Ex. 1007)
- The AT Attachment with Packet Interface - 6 Standard, Revision 3a ("Revision 3a of the ATA-6 Standard"), publicly available online as of January 2002 (Ex. 1008)

A. U.S. Patent No. 6,279,114 to Toombs et al. ("Toombs")

143. Toombs was filed on November 4, 1998, and was issued and published on August 21, 2001, one year and six months before the claimed priority date of the '486 Patent. Toombs qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a), (b), and (e).

144. Toombs incorporates by reference The MultiMediaCard System Specification, Version 1.4 by the MMCA Technical Committee ("MMC Specification"). Ex. 1005 at 31:18-22; Ex. 1010.

145. In general, Toombs describes a universal and detachable low cost data storage and communication system. Ex. 1005 at 1:6-8. Since designers face obstacles in allowing multicard systems to accept cards made from different vendors, an objective of Toombs is to solve problems such as "incapability of operating voltages, and error correction protocols, etc." *Id*. at 1:36-42.

146. Toombs describes a memory card comprising several memory locations for storing data. *Id*. at 10:22-34; Fig. 17A; Fig. 17B. The CSD register is responsible for providing information to the MultiMediaCard host on how to access the card content, including values defining data format, error correction type, maximum data access time, etc. *Id*. at 10: 24-29. These entries are coded as either R=readable, W=writeable once, or E=erasable (multiple writeable). *Id*. at 10:29-31.

147. The host can access the registers by issuing a specific set of commands. *Id*. at 9:45-55. Thus, a memory card according to Toombs is controlled by a command set including a plurality of commands, which are related to operations such as data read, data write, changing card status, or obtaining card information. *Id*. at FIGs. 38-44.

148. Toombs discloses block oriented commands for transferring data. In one embodiment described in Toombs, the basic unit of data transfer between the MultiMediaCard system is one byte. *Id*. at 27:28-29. All data transfer options which require a block size always define block lengths as integer multiples of bytes. *Id*. at 27:30-32. The READ_BL_LEN field of the CSD register determines the data block length. *Id*. at 11:5-9. The size of the memory block is defined in READ_BL_LEN. *Id*. at 11:34-35. The data block length can be computed as $2^{READ\_BL\_LEN}$. *Id*. at 11:7-8. The block length might therefore be in the range of 1, 2, 4, … 2048. Ex. 1005 at 11:8−9; Fig. 23. Table 25 of the MMC specification, incorporated by reference into Toombs, illustrates this parameter. Ex. 1010 at 55.

READ_BL_LEN	Block length	Remark
0	2^0 = 1 Byte	
1	2^1 = 2 Bytes	
.....		
11	2^{11} = 2048 Bytes	
12-15	reserved	

Table 25: Data block length

149. For example, where READ_BL_LEN=9, the data block length will be equal to 512 bytes. This data block size will be used as an example throughout the discussion of Toombs.

150. Toombs discloses a memory card that is a storage element, where the storage capacity of the card is computed using read-only values C_SIZE and READ_BL_LEN stored to the CSD register. Ex. 1005 at 11:45-60.

151. In one embodiment, Toombs describes a read-only value that indicates whether the partial block sizes can be used in block read commands. *Id*. at 11:10-13. When the READ_BL_PARTIAL=0, only the READ_BL_LEN block size can be used for block oriented data transfers. *Id*. at 11:13-15. On the other hand, when READ_BL_PARTIAL=1, smaller blocks can be used as well. *Id*. at 11:15-17.

152. Toombs further describes a read-only value that indicates whether partial block sizes can be used in the write block commands. *Id*. at 12:42-45. When WRITE_BL_PARTIAL=0, only the WRITE_BL_LEN block size can be used for block oriented data write. *Id*. at 12:45-47. On the other hand, when WRITE_BL_PARTIAL=1, the smaller blocks can be used as well. *Id*. at 12:47-49.

153. As discussed herein, Toombs anticipates claim 6, 8-11, 22, and 25-27 of the '486 Patent. In addition, Toombs, when combined with Dent, renders obvious claims 6, 8-11, 12, 22, 23, and 25-27 of the '486 Patent. In addition,

Toombs, when combined with PCMCIA, renders obvious claims 6, 8-11, 12, 22, 23, and 25-27 of the '486 Patent. In addition, Toombs, when combined with ATA-6, renders obvious claims 6, 8-11, 12, 22, 23, and 25-27 of the '486 Patent.

B. U.S. Patent No. 6,314,504 to Dent ("Dent")

154. Dent was filed on March 9, 1999, and was issued and published on November 6, 2001, one year and two months before the claimed priority date of the '486 Patent. Dent qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a), (b), (e).

155. Dent describes a processor architecture and associated method to improve efficiency of memory accesses and thereby reduce power consumption. Ex. 1006 at Abstract. Dent discloses that "high program efficiency is desirable" in "the interests of low power consumption for embedded, battery-powered applications." *Id*. at 1:60-62. To this end, Dent recognizes the "need for a new microcomputer architecture that is convenient to program, has much expanded addressed space, and yet is efficient on program memory utilization and power consumption for embedded applications." *Id*. at 1:62-67. Dent explains the desirability of expanding the available range of addresses without the use of additional addressing bits because the use of fewer bytes reduces power consumption. *Id*. at 2:2-8.

156. In one embodiment disclosed in Dent, index registers are employed in calculating an effective address for a memory-reference instruction. *Id*. at 6:1-3. The index registers are used for reading, manipulating, and storing data to memory, and may be any suitable length or may have variable lengths. *Id*. at 6:30-34. Each index register comprises a mode byte indicating how the register value shall be used. *Id*. at 6:3-5.

157. Dent discloses a system in which the most significant byte of each register contains mode bits which indicate how the register shall be used in forming the address memory. *Id*. at 7:1-3. Dent describes a memory system in which a microprocessor can use a fixed range of 31 address bits in one mode (byte mode) to address up to 2GB of memory. *Id*. at 7:7−10. This mode is indicated when the value of the most significant bit of the index register is equal to 0. *Id*. at 7:9-10.

158. Dent further discloses a second mode in which the memory system can use only 30 of those same address bits to address up to 4GB of memory. *Id*. at 7:22−24. This mode is indicated when the value of the most significant bit of the index register is equal to 1, which in turn indicates that the second most significant bit indicates the addressing mode for the remaining 30 bits. *Id*. at 7:15-17.

159. As discussed herein, Dent, when combined with Toombs, renders obvious claims 6, 8-11, 12, 22, 23, and 25-27 of the '486 Patent.

C. PC Card Standard, Volume 2 Electrical Specification ("PCMCIA")

160. PC Card Standard, Volume 2 Electrical Specification ("the PCMCIA standard") defines specifications for PC Cards and communications between PC Card and their hosts. PCMCIA bears a copyright date 1999 and was publicly available online from the Personal Computer Memory Card International Association (PCMCIA) website as of at least November 2001, one year and two months before the claimed priority date of the '486 Patent. Ex. 1015 at 1-3. The PCMCIA standard qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(a) and (b).

161. The "Wayback Machine" maintained by Internet Archive at archive.org confirms that PCMCIA standard was publicly available online from the Personal Computer Memory Card International Association (PCMCIA) website as of at least November 2001. Ex. 1007; Ex. 1015 at 1-3. The PC Card website homepage included a link presented on a tab entitled "About PCMCIA". Ex. 1015 at 524-525. The linked page was entitled "About PCMCIA" and included a link to "PC Card Standards." *Id*. at 526-528. The linked page was entitled "Detailed Overview of the PC Card Standard" and included the PCMCIA/PC Card Standard Release History, showing listing "PC Card Standard 7.0 Release" in

February 1999. *Id*. at 529-536. The previous linked page entitled "About PCMCIA" included another link directing users to a page where PC Card Standard could be "ordered through this site." *Id*. at 527. This linked page was entitled "Online Order Form" and enables purchase of the updated standard by both members (for $50) and non-members (for $299). *Id*. at 537-539. PCMCIA is therefore § 102(b) prior art.

162. The PCMCIA standard continues an evolutionary process by providing additional capabilities thereby expanding the variety of PC Cards that can be supports. Ex. 1007 at 1. This release evolved the capacities of the of the former memory interface in a number of ways. For example, the PCMCIA standard describes that the capabilities of 16-bit PC Cards have been expanded and now provide 16 bit and 26 addressing. *Id*. at 1. These modifications were made to support "an emerging class of applications which require higher performance." *Id*.

163. The 26 address signals at the PC Card connector can directly address only 64 MBytes of memory. *Id*. at 41. However, a set of Function Configuration Registers (consisting of four 16-bit Address Extension Registers or the Configuration Option Register) provides the means for an extended PC Card memory space containing as many as 2^{42} PC Card Common Memory locations." *Id*. at 41.

164. The PCMCIA standard also describes a Configuration Option register which is used to configure the card, provide an address extension to select a 64 MByte page of Common Memory, and to issue a soft reset to the card. *Id*. at 55. The Configuration Option register's Common Memory Address Extension field can serve to provide six extra address extension bits. *Id*. at 56. The six address extension bits when combined with the PC Cards 26 address signals (A[25::0]), would allow for the addressing of as much as 4 Gigabytes of Common Memory for PC Cards employing a 64 MByte paging architecture. *Id*. at 56.

165. As discussed herein, PCMCIA, when combined with Toombs, renders obvious claims 6, 8-11, 12, 22, 23, and 25-27 of the '486 Patent.

D. ATA-6

166. The AT Attachment with Packet Interface - 6 Standard, Revision 3a ("Revision 3a of the ATA-6 Standard") specifies the AT Attachment Interface between host systems and storage devices. Ex. 1008 at 1. This interface is used by CompactFlash storage devices. *Id*. at 3. Revision 3a of the ATA-6 Standard was publicly available online for free download from the T13 website as of at least January 2002. Ex. 1015 at 1-3. Accordingly, Revision 3a of the ATA-6 Standard qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and 102(b).

167. The "Wayback Machine" maintained by Internet Archive at archive.org confirms that Revision 3a of the ATA-6 Standard was publicly available online from the T13 website as of at least January 2002. Ex. 1008; Ex. 1015 at 1-3. T13 is a Technical Committee of Accreted Standards Committee NCITS. Ex. 1015 at 6. The T13 homepage included a list of project drafts created or maintained by T13, including a PDF link to "ATA/ATAPI - 6 revision 3a." *Id*. at 6-26; 13. The PDF document was the revision 3a of the ATA/ATAPI - 6 standard, and bears the revision date "14 December 2001" on the cover page. *Id*. at 28. This PDF document was available for free download as of at least January 2002. *Id*. at 13.

168. Further evidence that Revision 3a of the ATA-6 Standard was publicly available before the priority data of the '486 Patent is shown by U.S. Patent Publication 2003/0235408 to Silvester et al. ("the '408 Publication"). Ex. 1014. The '408 Publication was filed as U.S. Patent Application 10/183,875 on June 25, 2002 and published on December 15, 2003. The '408 Patent incorporates by reference Revision 3a of the ATA-6 Standard. Ex. 1014 at ¶ [0023]. This shows further evidence that Revision 3a of the ATA-6 Standard was publicly available to a person having ordinary skill in the art as of at least June 25, 2002, the filing date of the '486 Patent. Revision 3a of the ATA-6 Standard is therefore at least § 102(a) prior art.

169. Revision 3a of the ATA-6 Standard specifies the AT Attachment Interface between host systems and storage devices. *Id*. at 1. Revision 3a of the ATA-6 Standard describes a 48-bit address feature in addition to the standard 28-bit addressing. *Id*. at 51. The standard 28-bit addressing method is limited to addressing 137GB of memory. *Id*. at. 51. The optional 48-bit Address feature set described in Revision 3a of the ATA-6 Standard allows device capacity of up to approximately 144 petabytes. *Id*. A bit stored in a register on the storage device indicates whether 48-bit addressing is supported. Id. at 23. Revision 3a of the ATA-6 Standard thus describes a basic addressing method, wherein the card uses 28-bit addressing to address 137GB of memory, and an expanded addressing method, wherein the card uses 48-bit addressing to address 144 petabytes of memory.

IX. Ground 1: Toombs Anticipates Claims 6, 8-11, 22, and 25-27

A. Toombs Anticipates Claim 6

1. "A memory card comprising"

170. The preamble of claim 6 recites "[a] memory card comprising." To the extent the preamble is a limitation, it is taught by Toombs. For example, Toombs describes "the architecture of a MultiMediaCard card of a preferred embodiment according to the present invention." Ex. 1005 Toombs at FIG. 14.

171. Accordingly, Toombs discloses this claim limitation.

2. "several memory locations for storing data and in which memory card is stored at least one parameter, the memory card configured so that the number of memory locations of the memory card can be calculated on the basis of said at least one parameter"

172. The next limitation of claim 6 recites "several memory locations for storing data, and in which memory card is stored at least one parameter, the memory card configured so that the number of memory locations of the memory card can be calculated on the basis of said at least one parameter." This element is also taught by Toombs.

173. Toombs discloses a Card-Specific Data (CSD) register for storing values that provide information the the MultMediaCard host on how to access the card content. *Id*. at 10:22-34; Fig. 17. One value stored by the CSD register is the parameter C_SIZE. *Id*. at 11:45. The parameter C_SIZE is stored to the CSD register as a mantissa and an exponent, as shown in Figure 17A:

NAME	FIELD	WIDTH	CELL TYPE	CSD-SLICE
CSD STRUCTURE	CSD_STRUCTURE	2	R	[127:126]
MMC PROTOCOL VERSION	MMC_PROT	4	R	[125:122]
RESERVED	-	2	R	[121:120]
DATA READ ACCESS-TIME-1	TAAC	8	R	[119:112]
DATA READ ACCESS-TIME-2 IN CLK CYCLES (NSAC*100)	NSAC	8	R	[111:104]
MAX. DATA TRANSFER RATE	TRAN_SPEED	8	R	[103:96]
CARD COMMAND CLASSES	CCC	12	R	[95:84]
MAX. READ DATA BLOCK LENGTH	READ_BL_LEN	4	R	[83:80]
PARTIAL BLOCKS FOR READ ALLOWED	READ_BL_PARTIAL	1	R	[79:79]
WRITE BLOCK MISALIGNMENT	WRITE_BLK_MISALIGN	1	R	[78:78]
READ BLOCK MISALIGNMENT	READ_BLK_MISALIGN	1	R	[77:77]
DSR IMPLEMENTED	DSR_IMP	1	R	[76:76]
EXTERNAL V_{PP}	VPROG	2	R	[75:74]
DEVICE SIZE MANTISSA	C_SIZE_MANT	8	R	[73:66]
DEVICE SIZE EXPONENT	C_SIZE_EXP	4	R	[65:62]
MAX. READ CURRENT @V_{DD} MIN	VDD_R_CURR_MIN	3	R	[61:59]
MAX. READ CURRENT @V_{DD} MAX	VDD_R_CURR_MAX	3	R	[58:56]

FIG. 17A

174. One of skill in the art would understand that C_SIZE is a single parameter expressed in terms of a mantissa and an exponent. Together, the 8-bit mantissa (C_SIZE_MANT) and the 4-bit exponent (C_SIZE_EXP) represent the parameter C_SIZE. Additionally, each of the mantissa and exponent are themselves parameters that are used as the basis for calculating the number of memory locations on the card.

175. In Toombs, the capacity of the card can be calculated on the basis of the parameter C_SIZE. Toombs discloses that the capacity of the memory card can be calculated by multiplying the number of memory blocks by the data

block length, where the data block length (BLOCK_LEN) can be computed as $2^{READ\_BL\_LEN}$. Ex. 1005 at 11:7-8. The block length (BLOCK_LEN) might therefor be in the range of 1, 2, 4 ... 2048 bytes. *Id*. at 11:8-9. The block length is multiplied by the number of blocks, which is a function of C_SIZE, to calculate the capacity of the memory card. This calculation is shown in column 11, lines 45-60 of Toombs:

> In the preferred embodiment, if the card is a storage element, the storage capacity of the card is computed from the entries C_SIZE, C_SIZE_MULT and READ_BL_LEN as follows:
>
> memory capacity = BLOCKNR * BLOCK_LEN
> where
> BLOCKNR = (C_SIZE+1) * MULT
> $MULT = 2^{C\_SIZE\_MULT+2}$ (C_SIZE_MULT < 8)
> $BLOCK\_LEN = 2^{READ\_BL\_LEN}$ (READ_BL_LEN < 12)
>
> Therefore, the maximal capacity in this preferred embodiment is 4096*512*2048=4 Gbytes. For example, a 4 Mbyte card with BLOCK_LEN=512 can be coded by C_SIZE_MULT=0 and C_SIZE=2047.

176. Toombs' disclosure of the parameter C_SIZE used to calculate the capacity of the memory card discloses "several memory locations for storing data, and in which memory card is stored at least one parameter, the memory card configured so that the number of memory locations of the memory card can be calculated on the basis of said at least one parameter."

3. "the memory card configured so that a specific number of bits is reserved for said at least one parameter"

177. The next limitation of claim 6 recites "the memory card configured so that a specific number of bits is reserved for said at least one parameter." This element is also taught by Toombs.

178. Toombs discloses reserving 12 bits (bits 62-73) of the CSD register for the C_SIZE parameter. Ex. 1005 at FIG. 17A. As described above, one of skill in the art would understand that C_SIZE is a parameter expressed in terms of a mantissa and an exponent. Together, the 8-bit mantissa (C_SIZE_MANT) and the 4-bit exponent (C_SIZE_EXP) represent the 12-bit parameter C_SIZE. Toombs' disclosure of reserving 12 bits of the CSD register for the C_SIZE parameter discloses "the memory card configured so that a specific number of bits is reserved for said at least one parameter." Moreover, both C_SIZE_MANT and C_SIZE_EXP are themselves parameters with reserved space in the CSD register that are used to calculate the number of memory locations in the card.

4. "the memory card further configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported"

179. The next limitation of claim 6 recites "the memory card further configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported." This element is also taught by Toombs.

180. Toombs discloses commands for transferring data. Ex. 1005 at 27:30-32. The basic unit of data transfer between the MultiMediaCard system is one byte. *Id*. at 27:28-29. Some transfer commands involve blocks of data, in which case the block size/length is defined as an integer multiple of bytes. *Id*. at 27:30-32, 43-44. The size of the block is the number of bytes which will be transferred when one data block is sent (or received) by the host. *Id*. at 27:44-46. The size of a block is either programmable or fixed, and information about the block sizes and the programmability is stored in the CSD. *Id*. at 27:47-49.

181. The maximum length for a data block is computed as $2^{READ\_BL\_LEN}$, where READ_BL_LEN is a value between 0-11. Ex. 1010 at 55. The block length might therefore be in the range 1, 2, 4...2048 bytes. Ex. 1005 at 11:5-9. The MMC Specification expressly describes that the data block length may be 512 bytes, where READ_BL_LEN=9 (2^9=512). Ex. 1010 at 55, 85. In the following discussion, a nominal data block length of 512 bytes is used.

182. The memory storage of the card described in Toombs is divided into physical memory blocks. *Id*. at 27:37-42. The size of each physical block of the card is defined by the READ_BL_LEN field of the CSD as well. Ex. 1010 at 27. Accordingly, the maximum *data* block that can be transferred with a single block command is equal to the size of a *physical* memory block of the card.

183. Toombs describes a single block read command (READ_SINGLE_BLOCK) referred to as CMD17. Ex. 1005 at 20:16-29; Fig. 39. This command reads a data block of the size selected by the SET_BLOCKLEN command (CMD16). *Id*. at Fig. 39. The default block length is specified in the CSD. *Id*.

184. The CSD further includes a READ_BL_PARTIAL field that indicates whether partial data blocks can be read with block read commands, such as CMD17. *Id*. at 11:10-13; FIG 17A. When the READ_BL_PARTIAL is not enabled, only data blocks of the size READ_BL_LEN can be used for block oriented data transfers. *Id*. at 11:13-15. Accordingly, when the READ_BL_PARTIAL field is set to "0", only data blocks of 512 bytes can be read. *Id*. But, when READ_BL_PARTIAL is enabled, smaller blocks can be read by the host as well. *Id*. at 11:15-17. Thus, when READ_BL_PARTIAL is set to "1," data blocks smaller than the 512 byte block size can be read. *Id*. at 11:15-17.

185. The size of a partial data block is set by the SET_BLOCKLEN command (CMD16), which specifies the smaller block size for subsequent commands. Ex. 1005 at 19:23-24; FIG. 39. In one example, CMD16 can be used to set SET_BLOCKLEN to 128 bytes, equivalent to 1/4 of the data block length defined by READ_BL_LEN discussed above. Alternatively, SET_BLOCKLEN may be 1 byte, equivalent to 1/512 of the data block length. *Id*.; Ex. 1005 at 12:48-

49. When read block partial is not enabled (READ_BL_PARTIAL=0), CMD16 will not allow the host to define block lengths smaller than READ_BL_LEN. In this case, the value set by SET_BLOCKLEN must be identical to READ_BL_LEN. *Id*.

186. Returning to the single block read command (CMD17) described in Toombs, the host is restricted to reading data blocks of length READ_BL_LEN, *e.g.*, 512 bytes, where READ_BL_PARTIAL is not enabled. *Id*. at 11:13-15. However, if read block partial is enabled, smaller blocks whose starting and ending address are entirely contained within one physical memory block, may also be transmitted. Ex. 1005 at 20:10-13. In this case, the single block read command (CMD17) reads a block of the size selected by the SET_BLOCKLEN (CMD16), which can be as small as one byte. *Id*. at 11:15-17, Fig. 39.

187. Accordingly, the bit indicating whether read block partial is enabled or not enabled is indicative of an addressing method because it indicates whether the memory card system can address data blocks of length READ_BL_LEN or data blocks smaller than READ_BL_LEN using CMD16. Toombs therefore discloses "the memory card further configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported."

188. Toombs also discloses a second example of "the memory card further configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported".

189. Toombs describes a stream write command, CMD20, that writes a stream of data to the card, beginning with a host-supplied starting address, and ending when the host issues a stop command. Ex. 1005 at 20:38-52.

190. The CSD of the card described in Toombs further includes a WRITE_BL_PARTIAL field that indicates whether partial data blocks can be written. *Id*. at 12:42-45, 20:44-48. When WRITE_BL_PARTIAL is set "the data stream can start and stop at any address within the card address space." *Id.* at 20:44-47. But, when WRITE_BL_PARTIAL is not enabled (set to "0"), "the data transfer starts and stops only at block boundaries." *Id.* Thus, as explained in *Toombs*:

> If a stream write operation is stopped prior to reaching the block boundary and partial block data transfer is allowed (as defined in the CSD), the part of the last block will be packed as a partial block and programmed. If partial blocks are not allowed, the remaining data will be discarded.

Ex. 1005 at 14:49-53.

191. Accordingly, the bit indicating whether write block partial is enabled or not enabled is addressing data indicative of an addressing method because it indicates whether the memory card system can address data "at any address within the card" or is limited to addressing data transfers to "start[] and

stop[] only at [physical] block boundaries." *Id.* 20:44-47. Toombs therefore discloses yet another example of "the memory card further configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported."

5. "wherein the addressing data indicates either a basic addressing method or an expanded addressing method"

192. The next limitation of claim 6 recites "wherein the addressing data indicates either a basic addressing method or an expanded addressing method." This element is also taught by Toombs.

193. As described with respect to the previous claim limitation, Toombs discloses a bit stored to the CSD register that indicates whether partial block reads are permitted.

194. In one addressing method, the memory card system does not permit partial block reads (READ_BL_PARTIAL=0), and the host can only read data blocks of length READ_BL_LEN. This is an expanded addressing method. In the example discussed above, the data block length defined by READ_BL_LEN of is 512 bytes. *Id*. When read block partial is not enabled, CMD16 must be identical to READ_BL_LEN. *Id*. Thus in the expanded addressing method described in Toombs, the smallest data block that can be read is READ_BL_LEN, *e.g.*, 512 bytes.

195. In another addressing method, the memory card system permits partial block reads (READ_BL_PARTIAL=1), and the host can read smaller data blocks of length SET_BLOCKLEN using CMD16. This is a basic addressing method.. When read block partial is enabled, CMD16 can be used by the host to access blocks smaller than READ_BL_LEN. Ex. 1005 at 11:10-18. In this basic addressing method, the host can set the value of SET_BLOCKLEN using CMD16, such that a single byte can be read with a block read command.

196. Toombs further discloses a second example of this claim limitation.

197. As described with respect to the previous claim limitation, the CSD register stores a bit that indicates whether partial block writes are permitted. This bit indicates whether the memory card system can address data "at any address within the card" or is limited to addressing data transfers to "start[] and stop[] only at [physical] block boundaries." *Id.* at 20:44-47; In this example, the "basic" method corresponds to the case where the partial writes are not permitted, and the start addresses (and stop addresses) are limited to the physical block boundaries. The "expanded" method corresponds to when partial writes are permitted, allowing the host to use "any address within the card" as the start and stop points for the transfer.

198. Toombs therefore discloses two examples of this claim limitation.

6. "wherein the expanded addressing method enables the addressing of data in a larger number of memory locations than the basic addressing method."

199. The final claim limitation of claim 6 recites "wherein the expanded addressing method enables the addressing of data in a larger number of memory locations than the basic addressing method."

200. As discussed with respect to the previous claim limitation, Toombs discloses addressing data indicative of either a basic addressing method or an expanded addressing method with a single bit that either enables or prohibits partial block reads.

201. Toombs discloses an expanded addressing method indicated by READ_BL_PARTIAL = 0 in which block lengths of READ_BL_LEN are used for block oriented data transfers. *Id*. As an example, the read block length may be set in the CSD register to be 512 bytes. *Id*. Accordingly, the expanded addressing method described in Toombs enables the addressing of data in each memory location of the 512 byte block. *Id*.

202. Toombs also discloses a basic addressing method indicated by READ_BL_PARITAL=1 in which the host can access subunits of READ_BL_LEN by using CMD16 to set SET_BLOCKLEN for block oriented

commands. For example, CMD16 can be used to set SET_BLOCKLEN as small as a single byte. Ex. 1005 at 11:17-18. This basic addressing method enables the addressing of data in a single memory location: the 1 byte subunit of the 512 byte READ_BL_LEN.

203. Accordingly, in this example in Toombs, the "expanded" addressing method enables addressing of data in a larger number of locations (512 byte locations) compared to the "basic" method, which enables addressing of data in a smaller number of locations (e.g. a single byte location). Toombs therefore discloses this claim limitation.

204. Toombs also discloses a second example of this claim element. As discussed in the previous claim element, write block partial being enabled (WRITE_BL_PARTIAL=1), corresponds to the "expanded" addressing method. In this mode, the host can invoke a stream write command and designate "any address" in the card at which to begin writing data, as opposed to the "basic" method, where the host is restricted to starting a write only at the physical block boundaries of the card. Accordingly, this "expanded" method enables the host to address a larger number of memory locations ("any address") compared to the basic addressing method (only the relatively smaller number of addresses corresponding to physical block boundaries are permitted).

205. Toombs therefore discloses two examples of this claim limitation. Ex. 1009 at ¶205; 207.

206. Because Toombs discloses each and every element of claim 6, Toombs anticipates claim 6.

B. Toombs Anticipates Claim 8

207. Dependent claim 8 of the '486 Patent recites "[a] memory card according to claim 6, comprising a bus connection block for connecting the memory card to a device and for transferring data between the device and the memory card." Toombs discloses all the limitations of claim 8.

208. Toombs describes that the MultiMediaCard bus connects the MultiMediaCard host to a MultiMediaCard card comprising various an I/O device. Ex. 1005 at 6:61-65. FIG. 4 of Toombs shows a MultiMediaCard bus system:

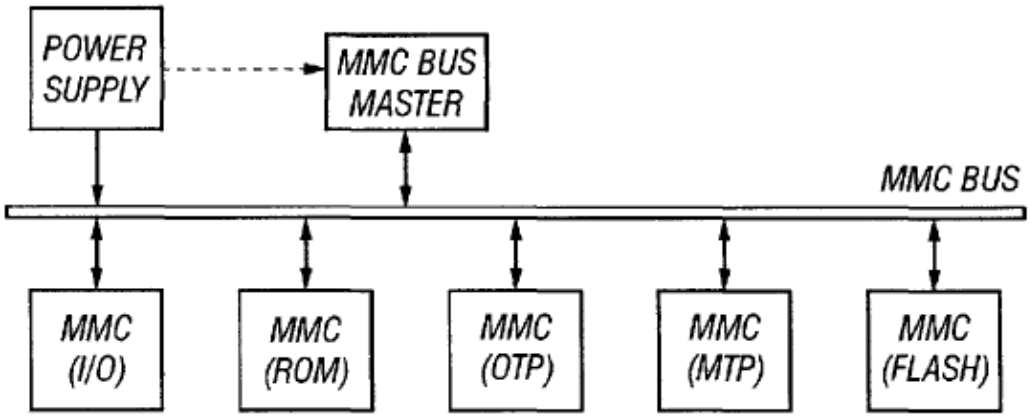


FIG. 4

209. Toombs describes that [i]n this MultiMediaCard bus protocol, the payload data transfer between the host and the cards is specifically designed to be bidirectional so that data can be transferred between the host to the cards." *Id*. at 7:14-17. The memory card interfaces with the MMC Interface Controller, as shown in FIG. 14 of Toombs:

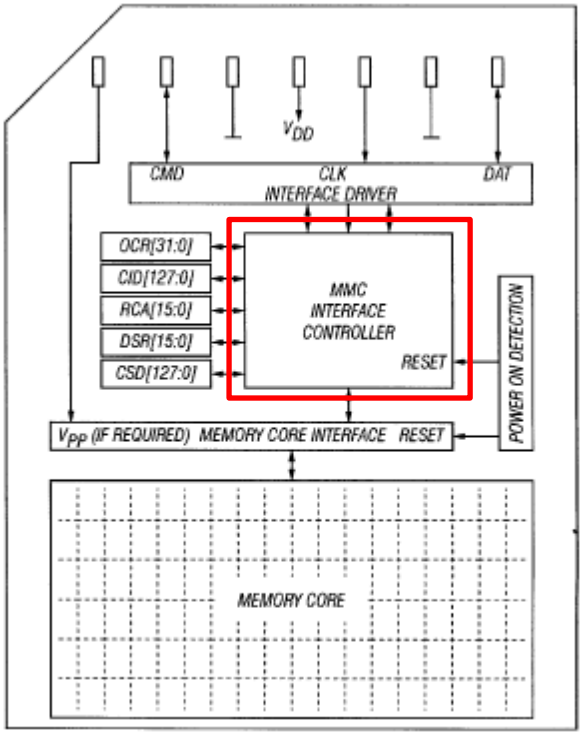


FIG. 14

210. Toombs therefore discloses "[a] memory card according to claim 6, comprising a bus connection block for connection the memory card to a device and for transferring data between the device and the memory card."

211. Toombs therefore discloses this claim limitation.

C. Toombs Anticipates Claim 9

212. Dependent claim 9 recites "[a] memory card according to claim 6, wherein data is arranged to be stored and read in the memory card block-by-block." Toombs discloses all the limitations of claim 9.

213. Toombs describes that the memory card system uses sequential command and block oriented commands. Ex. 1005 at 8:32-34. Both read and write operations allow either single or multiple block transmission. *Id*. at 8:46-48.

214. For example, Toombs discloses a write block command, CMD24, which writes a block of the size selected by the SET_BLOCKLEN command, assuming that write block partial is enabled. *Id*. at FIG. 41 (below).

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD24	ADTC	[31:0] DATA ADDRESS	R1B	WRITE_BLOCK	WRITES A BLOCK OF THE SIZE SELECTED BY THE SET_BLOCKLEN COMMAND.[1]
CMD25	ADTC	[31:0] DATA ADDRESS	R1B	WRITE_MULTIPLE_ BLOCK	CONTINUOUSLY WRITES BLOCKS OF DATA UNTIL A STOP_TRANSMISSION FOLLOWS.
CMD26	ADTC	[31:0] STUFF BITS	R1B	PROGRAM_CID	PROGRAMMING OF THE CARD IDENTIFICATION REGISTER. THIS COMMAND SHALL BE ISSUED ONLY ONCE PER MMC CARD. THE CARD CONTAINS HARDWARE TO PREVENT THIS OPERATION AFTER THE FIRST PROGRAMMING. NORMALLY THIS COMMAND IS RESERVED FOR THE MANUFACTURER.
CMD27	ADTC	[31:0] STUFF BITS	R1B	PROGRAM_CSD	PROGRAMMING OF THE PROGRAMMABLE BITS OF THE CSD.

FIG. 41

215. Toombs describes that WRITE_BL_LEN is used to indicate the block length for write operations. Ex. 1005 at 12:38-40. When write block partial is not enabled, only the WRITE_BL_LEN block size can be used for block oriented data write. *Id*. at 12:45-47.

216. Toombs describes that WRITE_BL_LEN is used to indicate the block length for write operations. Ex. 1005 at 12:38-40. When write block partial

is not enabled, only the WRITE_BL_LEN block size can be used for block oriented data write. *Id*. at 12:45-47. Toombs similarly describes block oriented commands that enable data to be read out of the card block-by-block. Toombs therefore discloses this claim limitation.

217. Because Toombs discloses each and every element of claim 9, it anticipates claim 9.

D. Toombs Anticipates Claim 10

218. Dependent claim 10 of the '486 Patent recites "[a] memory card according to claim 9, wherein the memory locations of one block are arranged to be addressed with one address." Toombs discloses all the limitations of claim 10.

219. Toombs discloses a write block command, CMD24. Ex. 1005 at FIG. 41. The write block command (CMD24) functions to write a block of the size selected by the SET_BLOCKLEN command. *Id*. The WRITE_BL_LEN of the preferred embodiment according to Toombs is used to indicate the block length for write operations. *Id*. at 12:38−41. The card receives one address as the argument, and programs the block of data into a location of memory starting with the address received as the command argument. *Id.* at 22:11-15, FIG. 41.

220. Toombs similarly describes block oriented commands that enable multiple blocks of data to be read using a single starting address. For example, CMD17 can be used to read a single data block from the card memory

using the starting address as the argument. Ex. 1005 at FIG. 39. Toombs therefore discloses this claim limitation.

221. Because Toombs discloses each and every element of claim 10, it anticipates claim 10.

E. Toombs Anticipates Claim 11

222. Dependent claim 11 of the '486 Patent recites "[a] memory card according to claim 9, wherein the memory card is a memory card according to MultiMediaCard specifications." Toombs discloses all the limitations of claim 11.

223. Toombs describes a MultiMediaCard in accordance with the specification, including the use of a MMC bus, "Serial Bus (MMC)," as well as various "MMC Adapters" to connect the host devices to MMC cards. Ex. 1005 at FIG. 1.

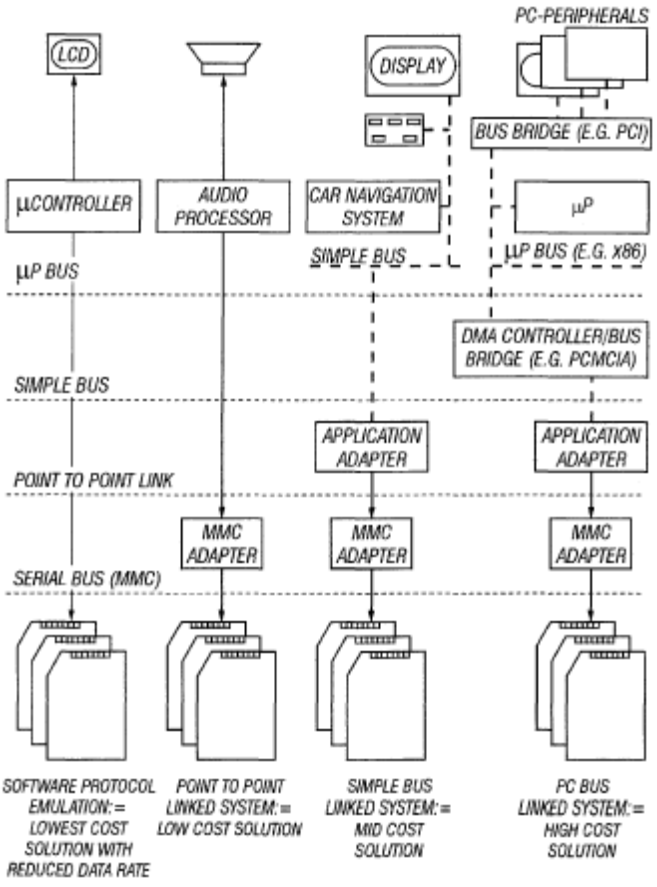


FIG. 1

224. Accordingly, Toombs discloses "[a] memory card according to claim 9, wherein the memory card is a memory card according to MultiMediaCard specifications."

225. Because Toombs discloses each and every element of claim 11, it anticipates claim 11.

F. Toombs Anticipates Claim 22

226. Dependent claim 22 recites "[a] memory card according to claim 6, wherein the basic addressing method supports addressing only one

memory location with one address." Toombs discloses all the limitations of claim 11.

227. As discussed above with respect to Claim 6, Toombs describes a basic addressing method indicated by the bit enabling partial block reads (READ_BL_PARTIAL=1). When partial block reads are permitted, the CMD16 can be used to set SET_BLOCKLEN as small as one byte such that single bytes can be read by the host. Ex. 1005 at 12:48-49. Accordingly, a single memory location, in this case one byte, can be read with one address, *i.e.* the address of the 1 byte block.

228. Because Toombs discloses each and every element of claim 22, it anticipates claim 22.

G. Toombs Anticipates Claim 25

229. Dependent claim 25 recites "[t]he memory card according to claim 6, wherein the memory card is configured so that, if the addressing data indicated that the memory card supports the expanded addressing method, the memory card uses the expanded addressing method in response to a successful reading of the addressing data that indicated support of the expanded addressing method." Toombs discloses all the limitations of claim 11.

230. As discussed in with respect to claim 6, Toombs describes an expanded addressing method indicated by the READ_BL_PARTIAL setting.

Toombs explains that in the setup procedure, command CMD9 is used to read the contents of the CSD register to obtain, e.g. block length, card storage capacity, etc. Ex. 1005 at 18:42-45, 24:34-35. When the host reads a "0" in the READ_BL_PARTIAL field of the CSD register, it will use the expanded addressing method. *Id*.

231. Moreover, as discussed in Section VII.A.a, Toombs describes an expanded addressed method indicated by WRITE_BL_PARTIAL=1 (i.e. partial writes are supported) in the CSD. When a host reads a "1" in the WRITE_BL_PARTIAL field of the CSD register, it can use the expanded addressing method, and invoke stream writing without regard to whether the start and stop points in the card address space correspond to physical block boundaries. Ex. 1005 at 20:44-47.

232. A POSITA would understand that CMD9 must be used before any addressing method can be used. Toombs explains that in the setup procedure, command CMD9 is used to read the contents of the CSD register to obtain the card Specific Data from its CSD register, e.g. block length, card storage capacity, and maximum clock rate, etc.. Ex. 1005 at 18:42-45. The contents of the CSD register are send as a response to CMD9. *Id*. at 24:36-37. The card must read the contents of the CSD register in order to know various parameters, including whether

READ_BL_PARTIAL and WRITE_BL_PARTIAL are set to 1 or to 0. Toombs therefore discloses this claim limitation.

233. Because Toombs discloses each and every element of claim 25, it anticipates claim 25.

H. Toombs Anticipates Claim 26

234. Dependent claim 26 of the '486 Patent recites "[a] memory card according to claim 6, further comprising a register for storing the addressing data." Toombs discloses all the limitations of claim 26.

235. Toombs discloses a Card-Specific Data register (CSD) "responsible for providing information to the MultiMediaCard host on how to access the card content." Ex. 1005 at 10:24-25. Specifically, "the CSD register stores values defining the data format. *Id*. at 10:22-33. One value stored in the CSD register is the bit that indicates whether read block partial is enabled. *Id*. at FIG. 17A.

236. In another example disclosed in Toombs, the CSD stores a bit that indicates whether write block partial is enabled. Ex. 1005 at FIG. 17B. Each of these bits are independently "addressing data." Accordingly, Toombs discloses "[a] memory card according to claim 6, further comprising a register for storing the addressing data."

237. Because Toombs discloses each and every element of claim 26, it anticipates claim 26.

I. Toombs Anticipates Claim 27

238. Dependent claim 27 of the '486 Patent recites "[a] memory card according to claim 26, wherein the stored addressing data comprises one bit." Toombs discloses all the limitations of claim 27.

239. Both READ_BL_PARTIAL and WRITE_BL_PARTIAL, which each independently constitute the stored addressing data, are single-bit settings in the CSD register (i.e. "Width = 1"). Excerpts from Figures 17A and 17B of Toombs illustrate this:

NAME	FIELD	WIDTH	CELL TYPE	CSD-SLICE
PARTIAL BLOCKS FOR READ ALLOWED	READ_BL_PARTIAL	1	R	[79:79]
PARTIAL BLOCKS FOR WRITE ALLOWED	WRITE_BL_PARTIAL	1	R	[21:21]

Toombs FIGs. 17A and 17B (excerpts).

240. Toombs therefore discloses this claim limitation.

241. Because Toombs discloses each and every element of claim 27, it anticipates claim 27.

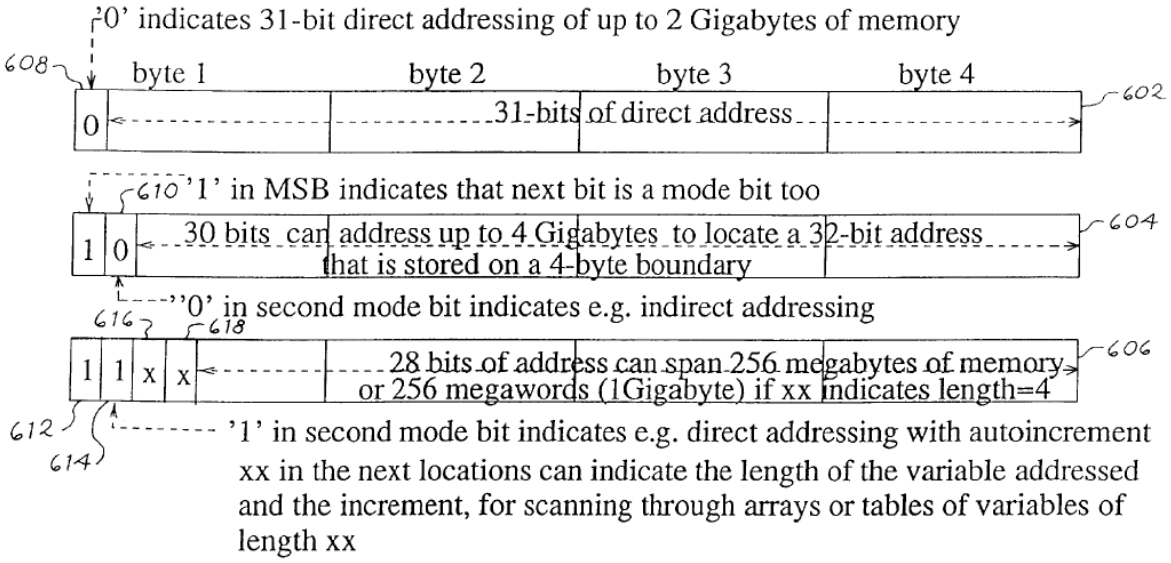
X. Ground 2: Toombs in View of Dent Renders Obvious Claims 6, 8-11, 22, 23, and 25-27

A. Toombs in View of Dent Renders Obvious Claim 6

242. To the extent that the Board finds that Toombs does not render claim 6 invalid as anticipated, this claim would be obvious over Toombs in view of Dent.

243. To the extent that the Board determines that Toombs does not disclose a "memory card configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported," this element would have been obvious in view of Dent. Dent discloses a processor architecture and associated method in which the most significant byte of an index register contains mode bits which indicate how the register shall be used in forming the address memory. Ex. 1006 at FID. 6; 7:1-3. In Dent, index registers are employed in calculating an effective address for a memory-reference instruction. *Id*. at 6:1-3. The index registers are used for reading, manipulating, and storing data to memory. *Id*. at 6:30-34. Each index register comprises a mode byte indicating how the register value shall be used. *Id*. at 6:3-5. Figure 6 of Dent illustrates how the most significant byte of an index register indicates an addressing method:

Fig. 6



244. Dent describes two modes by which the index registers can use the same number of address bits to be used to access differing amounts of memory. *Id*. Dent explains the desirability of expanding the available range of addresses without the use of additional address bits because the use of fewer bits reduces power consumption. *Id*. at 2:2-8. In one embodiment described in Dent, a microprocessor can use 31 address bits in "byte mode," to address up to 2GB of memory on a single-byte basis. *Id*. at 7:7-10. This first mode is indicated when the value of the most significant bit of the index register is equal to 0. *Id*.

245. In a second mode described in Dent, the microprocessor can use only 30 of those same address bits to address up to 4GB of memory on a 4-byte basis. *Id*. at 7:22-24. This second mode is indicated when the value of the most significant bit of the index register is equal to 1, which in turn indicates that the

second most significant bit is a mode bit as well. *Id*. at 7:15-17. Dent therefore discloses this limitation.

246. To the extent that the Board determines that Toombs does not disclose "the addressing data indicates either a basic addressing method or an expanded addressing method," this element would have been obvious over Toombs in view of Dent. Dent offers two modes that permit the same number of address bits to be used to access differing amounts of memory. Dent describes a memory system in which a microprocessor can use a fixed range of 31 address bits in one mode, single byte mode, to address up to 2GB of memory. Ex. 1006 at FIG. 6. This mode is a basic addressing method. Dent also describes a second mode, 4-byte "word" mode, in which the microprocessor can use only 30 of those same address bits to address up to 4GB of memory. *Id*. This mode is an expanded addressing method. Dent therefore discloses this claim limitation.

247. To the extent that the Board determines that Toombs does not disclose "wherein the expanded addressing method enables the addressing of data in a larger number of memory locations that the basic addressing method," this element would have been obvious over Toombs in view of Dent. As discussed in reference to the previous claim element, Dent offers two modes that permit the same number of address bits to be used to access differing amounts of memory. Dent describes two modes that permit the same number of address bits to be used

to access differing amounts of memory. The basic addressing method disclosed in Dent enables a microprocessor to address data in 2GB of memory locations. The expanded addressing method disclosed in Dent enables a microprocessor to address data in 4GB of memory locations. The expanded addressing method therefore enables the addressing of data in a larger number of memory locations than the basic addressing method by enabling addressing of data in 4GB of memory instead of only 2GB of memory. Dent therefore discloses this claim limitation.

248. Because the combination of Toombs and Dent discloses or suggests each and every element of claim 6, such combination renders obvious claim 6.

B. Toombs in View of Dent Renders Obvious Claims 8-11

249. As shown above in *Sections IX.A.C-IX.A.E,* Toombs describes this claim limitation. *See*, *supra*, ¶¶207-225.

C. Toombs in View of Dent Renders Obvious Claim 22

250. Dependent claim 22 of the '486 Patent recites "[a] memory card according to claim 6, wherein the basic addressing method supports addressing only one memory location with one address." This claim is obvious over Toombs in view of Dent.

251. Dent describes a basic mode of addressing where 31 address bits address up to 2GB of memory. Ex. 1006 7:7-9. A POSITA would understand that this teaches that each address corresponds to one byte (2^{31} = 2 gigabytes). Accordingly, each address in the basic addressing method described in Dent corresponds to and can be used to access the location of a single byte memory location. *Id*.

252. Because the combination of Toombs and Dent discloses or suggests each and every element of claim 22, such combination renders obvious claim 22.

D. Toombs in View of Dent Renders Obvious Claim 23

253. Claim 23 of the '486 Patent recites "[a] memory card according to claim 6, wherein the expanded addressing method supports a higher memory capacity than the basic addressing method." This claim is obvious over Toombs in view of Dent.

254. Dent offers two modes that permit the same number of address bits to be used to access differing amounts of memory. The basic addressing method addresses data in 2GB of memory locations. Ex. 1006 FIG. 6. The expanded addressing method disclosed in Dent enables addressing data in 4GB of memory locations. Ex. 1006 FIG. 6. The expanded addressing method described in

Dent therefore supports a higher memory capacity that the basic addressing method.

255. Because the combination of Toombs and Dent discloses or suggests each and every element of claim 23, such combination renders obvious claim 23.

E. Toombs in View of Dent Renders Obvious Claim 25

256. Claim 25 of the '486 Patent recites "[a] memory card according to claim 6, wherein the memory card is configured so that, if the addressing data indicated that the memory card supports the expanded addressing method, the memory card uses the expanded addressing method in response to a successful reading of the addressing data that indicated support of the expanded addressing method." This claim is obvious over Toombs in view of Dent.

257. Dent discloses an expanded addressing method to address up to 4GB of memory. The most significant byte of the index register contains mode bits which indicate how the register is to be interpreted in addressing the memory. *Id*.; Ex. 1006 7:1-3. The expanded addressing method is indicated in the first byte of the 32 bit address stored to an index register. Ex. 1009 ¶281.

258. A POSITA would understand that the most significant byte of the index register must be successfully read by the microprocessor before an

expanded addressing method as described in Dent can be used. Dent therefore discloses this claim limitation.

259. Because the combination of Toombs and Dent discloses or suggests each and every element of claim 25, such combination renders obvious claim 25.

F. Toombs in View of Dent Renders Obvious Claim 26

260. Claim 26 of the '486 Patent recites "[a] memory card according to claim 6, further comprising a register for storing the addressing data." This claim is obvious over Toombs in view of Dent.

261. Dent describes addressing mode bits that are indicative of an addressing method. Figure 6 of Dent "shows formatting for index registers using addressing mode bits." Ex. 1006 2:23-24. Dent therefore discloses a register for storing the addressing data.

262. Because the combination of Toombs and Dent discloses or suggests each and every element of claim 26, such combination renders obvious claim 26.

G. Toombs in View of Dent Renders Obvious Claim 27

263. Claim 27 of the '486 Patent recites "[a] memory card according to claim 26, wherein the stored addressing data comprises one bit." This claim is obvious over Toombs in view of Dent.

264. Dent discloses addressing data stored to a register that indicates a basic addressing method or an expanded addressing method. Ex. 1006 FIG. 6. The value 0 in the most significant bit of the index register indicates a basic mode of addressing. *Id*. Therefore, the single, first bit of the index register constitutes addressing data.

265. It would also be obvious to modify Dent such that a value of 1 in the most significant bit of the index register would identify the expanded mode of addressing. In Dent's expanded mode, the system uses the first 2 bits of data to identify the expanded mode (the second bit is used to distinguish between the expanded mode and a third addressing mode involving an auto-incrementing addressing feature), and uses the remaining 30 of the address bits to address up to 4 GB of memory using 4-byte word addressing. *Id*.; Ex. 1006 7:22−24, FIG. 6.

266. A POSITA would find it obvious to simplify Dent to use only two addressing modes, distinguished by a single bit in the addressing data stored to the index register. This simplification would permit a single bit that indicates either a basic addressing method that permits byte addressing of 2 GB (2^{31} addresses * 1 Byte/address), or an expanded addressing method that permits word addressing allowing increased memory capacity, for example addressing of 4GB (2^{31} addresses) * (2 Byte/address). *Id*. A POSITA would be motivated to make this simplification, eliminating the third addressing mode of Dent, to permit an

additional bit to be used for the address data. *Id*. This would permit a larger number of discrete addresses to be used by the host in the expanded access mode (31 bits versus 30 in Dent), allowing the host more granular access to the stored data. *Id*.

267. A POSITA, in view of Dent's teachings, would recognize the benefit to this approach, which maintains the same number of total bits (32 in the case of Dent) used to convey addressing information, while permitting the host to address larger total memory capacities. Ex. 1009 ¶290. This would avoid the need to redesign the interface addressing interface between the host and the memory device, while still permitting the host to take advantage or larger capacity memory devices. *Id*. Moreover, a POSITA would recognize this approach would allow the system designer to easily expand this system to access larger memory arrays by simply enlarging the size of the word (i.e. the number of bytes in memory accessed with a single address). *Id*..

268. Furthermore, this claim element uses the open term "comprises" rather than a closed term, such as "consisting of." The term "comprises one bit" means "at least one bit" so if there is or more bits stored to a register, this limitation is satisfied.

269. Because the combination of Toombs and Dent discloses or suggests each and every element of claim 27, such combination renders obvious claim 27.

H. Motivation to Combine Toombs and Dent

270. A POSITA would have been motivated to combine Toombs with the teachings of Dent to achieve a memory card capable of expanded addressing. Toombs and Dent are analogous references as they relate to techniques for accessing digital memory and both suggest the desirability of providing a low power memory system that offers high performance while allowing for access to an expanded number of memory locations as card size grows. *Id*. Indeed, both Toombs and Dent describe the respective inventions with reference to applications of memory access in, for example, mobile phones. Ex. 1005 at 1:19-42; Ex. 1006 at 1:46-67.

271. It would have been obvious to a POSITA to apply Dent's technique of using index register bits to determine an addressing method to the system described in Toombs in order to enable a memory card to operate in a basic or expanded addressing method, depending on the card size. Toombs describes that it uses 32-bit addresses to indicate the address of a byte stored in the memory. Ex. 1005 at Fig. 41 (CMD 24 and CMD17 access a block of the size selected by the SET_BLOCKLEN). In the case of sequential reads, Toombs also discloses the use

of the 32-bit address to indicate the first byte of a stream of data. Ex. 1005 at 97. A POSITA would recognize that this addressing method presents a limit as to the size of the address space (in bytes).

272. The express teaching in Dent provides motivation to use its addressing modes to permit greater addressing with fewer bytes, and therefore with lower power, to increase capacity. Ex. 1006 at 1:57-67. A POSITA would have been motivated to consider different versions of memory storage and addressing, such as microprocessor memory system taught in Dent, to enable different addressing methods in a memory card as described in Toombs. To this end, a POSITA would be motivated to use a stored bit (or bits) to determine an effective address for a memory reference location, as described in Dent, to the memory card described in Toombs.

273. Further, a POSITA would recognize that the definition or value of a parameter such as C_SIZE could be changed so that it related to the larger blocks of data that an expanded device would address and could continue to be used to calculate the capacity of the expanded memory card. Alternatively, if capacity increased and the C_SIZE parameter functioned the same way, a POSITA would consider adding more bits for the parameter C_SIZE to accommodate the increased address space. This combination would also yield a predictable result — a memory card with addressing modes that accommodate greater addressing with

fewer bytes, and therefore with lower power, such that capacity of the memory card is increased.

XI. Ground 3: Toombs in View of PCMCIA Renders Obvious Claims 6, 8-11, 22, 23, and 25-27

A. Toombs in View of PCMCIA Renders Obvious Claim 6

274. To the extent that the Board finds that Toombs does not render claim 6 invalid as anticipated, this claim would be obvious over Toombs in view of PCMCIA.

275. To the extent that the Board determines that Toombs does not disclose a "memory card configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported," this element would have been obvious in view of PCMCIA.

276. PCMCIA defines specifications for PC Cards and communications to and from hosts. Ex. 1007 at 1. PCMCIA describes multiple ways of expanding addressing for a PC card memory system. One way is the use of additional address bits.

277. PCMCIA describes a Configuration Option register which is used to configure the card and provide an address extension to select a 64 MB page of Common Memory. Ex. 1007 at 55. The Configuration Option register's Common Memory Address Extension field provides six address extension bits, as shown in Table 4-29 below. Id. at Table 4-29; 56.

Table 4–29 Configuration Option Register

D7	D6	D5	D4	D3	D2	D1	D0
SRESET	LevlREQ	Function Configuration Index / Common Memory Address Extension					

Common Memory Address Extension	R/W	For a memory card with > 64 MBytes of Common Memory and using 64 MByte paging this field can be used to provide six address extension bits which select a 64 MByte page within a Common Memory space as large as 4 Gigabytes. The selection of the Common Memory Address Extension field option for use with 64 MByte paging as well as the exact size of Common Memory is specified by the CISTPL_EXTDEVICE tuple.

278. The selection of the Common Memory Address Extension field option for use with 64MByte paging as well as the exact size of Common Memory is specified by the CISTPL_EXTDEVICE tuple. *Id*.at Table 4-29; 56. This tuple is contained in the memory card's Card Information Structure, which is stored in the attribute memory of the card. *Id*. at 1; 15. This tuple is therefore addressing data indicative of at least one supported addressing method.

279. Another means of expanding capacity described in PCMCIA is an optional set of Function Configuration Registers that provide a means for a system to access more than 64 MBytes of Common Memory space on a PC card. Ex. 1007 at 63. The 26 address signals at the PC Card connector can directly access only 64 MBytes of memory. *Id*. The Address Extension Registers provide an address extension which allows the host system to address locations within an extended PC Card memory space containing as many as 2^{42} PC Card Memory locations with 8-bit registers. *Id*.

280. With regard to the Common Memory Address Extension field, the CISTPL_EXTDEVICE tuple stored to the memory card is addressing data

indicative of at least one addressing method supported. Further, this data is indicative of either a basic addressing method or an expanded addressing method. PCMCIA discloses a basic addressing method, wherein the card neither contains an Address Extension Register nor uses the Configuration Option Register for address extension. *Id*. at 14; Table 4-3. PCMCIA also discloses an expanded addressing method, wherein the card uses the Configuration Option Register for address extension. *Id*.

281. The basic addressing method disclosed in PCMCIA enables addressing of 64MB of memory. *Id*. The expanded addressing method disclosed in PCMCIA enables addressing of 4 Gigabytes of memory. *Id*. PCMCIA therefore discloses an expanded addressing method which enables the addressing of data in a larger number of memory locations than the basic addressing method.

282. Because the combination of Toombs and PCMCIA discloses or suggests each and every element of claim 6, such combination renders obvious claim 6.

B. Toombs in View of PCMCIA Renders Obvious Claim 8-11

283. As shown above in *Sections IX.A.C-IX.A.E,* Toombs describes this claim limitation. *See*, *supra*, ¶¶207-225.

C. Toombs in View of PCMCIA Renders Obvious Claim 22

284. Claim 22 of the ’486 Patent recites “[a] memory card according to claim 6, wherein the basic addressing method supports addressing only one memory location with one address.” This claim is obvious over Toombs in view of PCMCIA.

285. PCMCIA describes a memory card with basic addressing method which uses 2^{26} addresses (signals A[25::0]) to address a memory of 64MB. Ex. 1007 at Table 4-3. A POSITA would recognize that 2^26= 67,108,864 bytes * 1MB/2^20 bytes = 64MB. Ex. 1009 at ¶325. Accordingly, each address in the basic addressing method described in PCMCIA can access a single memory location (i.e. a single byte).

286. Because the combination of Toombs and PCMCIA discloses or suggests each and every element of claim 22, such combination renders obvious claim 22.

D. Toombs in View of PCMCIA Renders Obvious Claim 23

287. Claim 23 of the ’486 Patent recites “[a] memory card according to claim 6, wherein the expanded addressing method supports a higher memory capacity than the basic addressing method.” This claim is obvious over Toombs in view of PCMCIA.

288. As discussed in reference to claim 6, PCMCIA discloses addressing data indicative of a basic addressing method or an expanded addressing

method. The PCMCIA standard describes a Configuration Option register which is used to configure the card, provide an address extension to select a 64 MByte page of Common Memory, and to issue a soft reset to the card. Ex. 1007 at 55. The Configuration Option register's Common Memory Address Extension field can serve to provide six extra address extension bits. *Id*. at 56. The six address extension bits when combined with the PC Cards 26 address signals (A[25::0]), would allow for the addressing of as much as 4 Gigabytes of Common Memory for PC Cards employing a 64 MByte paging architecture. *Id*. at 56; Table 4-29 (below).

Table 4–29 Configuration Option Register

D7	D6	D5	D4	D3	D2	D1	D0
SRESET	LevlREQ	Function Configuration Index / Common Memory Address Extension					

Common Memory Address Extension	R/W	For a memory card with > 64 MBytes of Common Memory and using 64 MByte paging this field can be used to provide six address extension bits which select a 64 MByte page within a Common Memory space as large as 4 Gigabytes. The selection of the Common Memory Address Extension field option for use with 64 MByte paging as well as the exact size of Common Memory is specified by the CISTPL_EXTDEVICE tuple.

289. Accordingly, PCMCIA discloses a basic addressing method, wherein the card neither contains an Address Extension Register nor uses the Configuration Option Register for address extension. In this basic addressing method, the capacity of the PC card is 64 MB. *Id*. at 14. PCMCIA also discloses an expanded addressing method, wherein the card uses the Configuration Option Register for address extension. In this expanded addressing method, the capacity of the memory card is 4 GB. *Id*. at 56; Table 4-29. PCMCIA therefore discloses "[a]

memory card according to claim 6, wherein the expanded addressing method supports a higher memory capacity than the basic addressing method."

290. Because the combination of Toombs and PCMCIA discloses or suggests each and every element of claim 23, such combination renders obvious claim 23.

E. Toombs in View of PCMCIA Renders Obvious Claim 25

291. Claim 25 of the '486 Patent recites "[a] memory card according to claim 6, wherein the memory card is configured so that, if the addressing data indicated that the memory card supports the expanded addressing method, the memory card uses the expanded addressing method in response to a successful reading of the addressing data that indicated support of the expanded addressing method." This claim is obvious over Toombs in view of PCMCIA.

292. PCMCIA discloses an expanded addressing method wherein the Common Memory Address Extension field option is used with 64MB paging. Use of the Common Memory Address Extension field is specified by the CISTPL_EXTDEVICE tuple. Ex. 1007 at 56, Table 4-29. This tuple is stored in the memory card's Card Information Structure (CIS) in the attribute memory of the card. *Id*. at 1; 15. While in the power-up state, the PC card shall allow the card information structure to be read and Configuration registers to be accessed. *Id*. at 54.

293. A POSITA would understand that the CISTPL_EXTDEVICE must be successfully read by the microprocessor before an expanded addressing method as described in PCMCIA can be used.

294. Because the combination of Toombs and PCMCIA discloses or suggests each and every element of claim 25, such combination renders obvious claim 25.

F. Toombs in View of PCMCIA Renders Obvious Claim 26

295. Claim 26 of the '486 Patent recites "[a] memory card according to claim 6, further comprising a register for storing the addressing data." This claim is obvious over Toombs in view of Dent.

296. The addressing method is specified by the CISTPL_EXTDEVICE tuple. Ex. 1007 56, Table 4-29. The CISTPL_EXTDEVICE tuple is stored in the card information structure (CIS) in attribute memory. *Id*. at 1; 15; 167. A POSITA would understand that the card information structure is a register. The CIS of a PC Card stores tuples that identify functions and data formats for the card. *Id*. at 1. Accordingly, the CIS stores the addressing data of the CISTPL_EXTDEVICE that indicates whether the card supports a basic or an expanded addressing method.

297. To the extent that the CIS of the PC card is not a register, it would be obvious to modify the PC Card to store information about the functions

and data format of the card in a register, such as the CSD register of the MMC card described in Toombs. For at least the reasons described below, it would obvious to a POSITA to modify the memory card of PCMCIA to store information indicative of an addressing method in a register.

298. Because the combination of Toombs and PCMCIA discloses or suggests each and every element of claim 26, such combination renders obvious claim 26.

G. Toombs in View of PCMCIA Renders Obvious Claim 27

299. Claim 27 of the '486 Patent recites "[a] memory card according to claim 26, wherein the stored addressing data comprises one bit." This claim is obvious over Toombs in view of [PCMCIA?].

300. PCMCIA discloses a tuple stored to the in the card information structure (CIS) in attribute memory indicative of an expanded or basic addressing method.. It would be obvious to modify PCMCIA to store the addressing data as a single bit in the CIS in order to indicate whether the card supports expanded addressing to minimize the size of the register stack and increase processing speed.

301. To the extent that the CIS of the PC card is not a register, it would be obvious to modify the PC Card to store information about the functions and data format of the card in a register, such as the CSD register of the MMC card described in Toombs. For at least the reasons described in Section *VIII.C.h*, below,

it would obvious to a POSITA to modify the memory card of PCMCIA to store information indicative of an addressing method in a register.

302. Furthermore, this claim element uses the term "comprises." The term "comprises one bit" means "includes at least one bit" so if there is more than one bit stored to a register, this limitation is satisfied.

303. Because the combination of Toombs and PCMCIA discloses or suggests each and every element of claim 27, such combination renders obvious claim 27.

H. Motivation to Combine Toombs and PCMCIA

304. A POSITA would have been motivated to combine Toombs with the teachings of PCMCIA to achieve a memory card capable of expanded addressing. A POSITA would have recognized that the memory card described in Toombs could not address more than 2GB of data, and would have been motivated to consider how the other leading mass storage standards had solved this problem when they reached the limits of the addressing methods inherent in their design. The prior-art in mass storage devices, such as removable flash memory cards in the case of PCMCIA, encountered the same problem as Toombs of limited capacity. Therefore there was a known need for the capability to access a larger number of addresses than the original standards allowed.

305. In PCMCIA, the standard was expanded by increasing the number of address bits so that a larger number of addresses could be accessed. In order for a host to know whether a particular PCMCIA card used the expanded addressing method, or only worked with limited addressing of the original standard, a tuple was stored in the device so that the host could read that data and, based on that data, the host could know that it should use the expanded addressing method.

306. It would be obvious to a POSITA to store the information indicative of the addressing mode, i.e. the information indicating that a higher number of address bits are available, in a register, such as the CSD register described in Toombs. The CIS (card information structure) described in PCMCIA functions in the same manner as the CSD register of Toombs - it stores information about the functions and data format of the card so that the host can read the information and know the constraints of the memory card. Accordingly, a POSITA would have been motivated to substitute a register for a card information structure to achieve predictable results - easy access by the host to information about the card's function and format.

307. Further, a POSITA would understand that modifying Toombs with the teaching of PCMCIA would enable a memory system to be able to calculate the capacity of the card based on a stored parameter such as C_SIZE. It

would have been obvious to a POSITA to continue to use a parameter such as C_SIZE, and to expand the number of bits of the parameter to accommodate a larger capacity.

XII. Ground 4: Toombs in View of ATA-6 Renders Obvious Claims 6, 8-11, 22, 23, and 25-27

A. Toombs in View of ATA-6 Renders Obvious Claim 6

308. To the extent that the Board finds that Toombs does not render claim 6 invalid as anticipated, this claim would be obvious over Toombs in view of Revision 3a of the ATA-6 Standard.

309. To the extent that the Board determines that Toombs does not disclose a "memory card configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported," this element would have been obvious in view of Revision 3a of the ATA-6 Standard.

310. Revision 3a of the ATA-6 Standard specifies the AT Attachment Interface between host systems and storage devices. Ex. 1008 at 1. This interface is used by CompactFlash storage devices. *Id*. at 3. Revision 3a of the ATA-6 Standard describes a data register used for sending commands to the device or posting status from the device. *Id*. at 63. The IDENTIFY DEVICE command enables the host to receive parameter information from the device. *Id*. at 114. This command allows the host to read device identification data from Data register. *Id*.

Table 27 of Revision 3a of the ATA-6 Standard defines the arrangement and meaning of the parameter words in the buffer, shown below. *Id*. at 117.

Table 27 – IDENTIFY DEVICE information *(continued)*

Word	O/M	F/V		Description
81	M	F		Minor version number 0000h or FFFFh = device does not report version 0001h-FFFEh = see 8.15.41
82	M			Command set supported.
		X	15	Obsolete
		F	14	1 = NOP command supported
		F	13	1 = READ BUFFER command supported
		F	12	1 = WRITE BUFFER command supported
		X	11	Obsolete
		F	10	1 = Host Protected Area feature set supported
		F	9	1 = DEVICE RESET command supported
		F	8	1 = SERVICE interrupt supported
		F	7	1 = release interrupt supported
		F	6	1 = look-ahead supported
		F	5	1 = write cache supported
		F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3	1 = mandatory Power Management feature set supported
		F	2	1 = Removable Media feature set supported
		F	1	1 = Security Mode feature set supported
		F	0	1 = SMART feature set supported
83	M			Command sets supported.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13	1 = FLUSH CACHE EXT command supported
		F	12	1 = mandatory FLUSH CACHE command supported
		F	11	1 = Device Configuration Overlay feature set supported
		F	10	1 = 48-bit Address feature set supported
		F	9	1 = Automatic Acoustic Management feature set supported
		F	8	1 = SET MAX security extension supported
		F	7	See Address Offset Reserved Area Boot, NCITS TR27:2001
		F	6	1 = SET FEATURES subcommand required to spinup after power-up
		F	5	1 = Power-Up In Standby feature set supported
		F	4	1 = Removable Media Status Notification feature set supported
		F	3	1 = Advanced Power Management feature set supported
		F	2	1 = CFA feature set supported
		F	1	1 = READ/WRITE DMA QUEUED supported
		F	0	1 = DOWNLOAD MICROCODE command supported

311. Revision 3a of the ATA-6 Standard describes that bit 10 of word 83 of the device identification data indicates whether 48-bit addressing is supported. Ex. 1008 at 22-23, 117. This bit is addressing data indicative of at least one addressing method. If this field is not enabled, 28-bit addressing is supported. Accordingly, Revision 3a of the ATA-6 Standard discloses a "memory card

configured to have stored therein an addressing data, said addressing data being indicative of at least one addressing method supported."

312. To the extent that the Board determines that Toombs does not disclose a "wherein the addressing data indicates either a basic addressing method or an expanded addressing method," this element would have been obvious in view of Revision 3a of the ATA-6 Standard.

313. As discussed in reference to the previous claim element, Revision 3a of the ATA-6 Standard describes a bit in a Data register that indicates whether 48-bit addressing is supported. If this field is not enabled, 28-bit addressing is supported. The optional 48-bit address feature set allows devices with capabilities up to 281 tera sectors. Ex. 1008 at 51. A sector is a uniquely addressable set of 512 bytes. *Id*. at 5. This allows device capacity of up to approximately 144 petabytes. *Id*. at 51. Also described is a set of commands unique to the 48-bit address feature. *Id*. Accordingly, the addressing data, bit 10 of word 38 in the Data register, indicates that either the expanded addressing method (48-bit addressing) is enabled or that the basic addressing method (28-bit addressing) is enabled.

314. To the extent that the Board determines that Toombs does not disclose a "wherein the expanded addressing method enables the addressing data in

a larger number of memory locations than the basic addressing method," this element would have been obvious in view of Revision 3a of the ATA-6 Standard.

315. Revision 3a of the ATA-6 Standard describes a bit in a data register that indicates either an expanded or a basic addressing method. The expanded addressing method described in Revision 3a of the ATA-6 Standard allows a device to address approximately 144 petabytes. Ex. 1008 at 51. Where 48-bit addressing is not enabled, the device operates in a basic addressing method using 28-bit addresses. Id. In this basic addressing method, the device capacity is limited to 228 (268,435,456) sectors of 512 bytes each for a total of 137 gigabytes. The expanded addressing method described in Revision 3a of the ATA-6 Standard therefore enables the address of data in a larger number of memory locations that the basic addressing method.

316. Because the combination of Toombs and Revision 3a of the ATA-6 Standard discloses or suggests each and every element of claim 6, such combination renders obvious claim 6.

B. Toombs in View of ATA-6 Renders Obvious Claim 8-11

317. As shown above in *Sections IX.A.C-IX.A.E,* Toombs describes this claim limitation. *See*, *supra*, ¶¶207-225.

C. Toombs in View of ATA-6 Renders Obvious Claim 22

318. Claim 22 of the ’486 Patent recites “[a] memory card according to claim 6, wherein the basic addressing method supports addressing only one memory location with one address.” This claim is obvious over Toombs in view of Revision 3a of the ATA-6 Standard.

319. As discussed with reference to claim 6, Revision 3a of the ATA-6 Standard describes a basic addressing method that uses 28-bit addressing. In this basic addressing method, host command such as WRITE SECTOR address a sector, a uniquely addressable set of 512 bytes. Ex. 1008 at 5, 303. In a system that uses sector-based commands, reading or writing a single sector is equivalent to addressing a single memory location. A memory location does not correspond to a particular size or number of bits, as described in the ‘486 Patent. Ex. 1001 at 1:62-65. Accordingly, a WRITE SECTOR command addresses a single memory location (one sector) with one address (the starting address of the sector to be written). Ex. 1008 at 303.

320. Because the combination of Toombs and Revision 3a of the ATA-6 Standard discloses or suggests each and every element of claim 22, such combination renders obvious claim 22.

D. Toombs in View of ATA-6 Renders Obvious Claim 23

321. Claim 23 of the ’486 Patent recites “[a] memory card according to claim 6, wherein the expanded addressing method supports a higher memory

capacity than the basic addressing method." This claim is obvious over Toombs in view of Revision 3a of the Revision 3a of the ATA-6 Standard.

322. As discussed in reference to Claim 6, Revision 3a of the ATA-6 Standard describes a bit in a data register that indicates either an expanded or a basic addressing method. The expanded addressing method described in Revision 3a of the ATA-6 Standard allows a device to address approximately 144 petabytes. Ex. 1008 at 51. Where 48-bit addressing is not enabled, the device operates in a basic addressing method using 28-bit addresses. *Id*. In this basic addressing method, the device capacity is limited to 228 (268,435,456) sectors of 512 bytes each for a total of 137 gigabytes. *Id*. The expanded addressing method described in ATA-6 therefore supports a higher memory capacity than the basic addressing method. Accordingly, Revision 3a of the ATA-6 Standard discloses "[a] memory card according to claim 6, wherein the expanded addressing method supports a higher memory capacity than the basic addressing method."

323. Because the combination of Toombs and Revision 3a of the ATA-6 Standard discloses or suggests each and every element of claim 23, such combination renders obvious claim 23.

E. Toombs in View of ATA-6 Renders Obvious Claim 25

324. Claim 25 of the '486 Patent recites "[a] memory card according to claim 6, wherein the memory card is configured so that, if the addressing data

indicated that the memory card supports the expanded addressing method, the memory card uses the expanded addressing method in response to a successful reading of the addressing data that indicated support of the expanded addressing method." This claim is obvious over Toombs in view of ATA-6.

325. Revision 3a of the ATA-6 Standard describes a data register that stores addressing data indicative of an expanded or basic addressing method. The IDENTIFY DEVICE command enables the host to receive parameter information from the device. Ex. 1008 at 114. This command allows the host to read the 256 words of device identification data from Data register, including bit 10 of word 38 which indicates an addressing method. *Id*.

326. A POSITA would understand that the device identification information in the Data Register must be read by the host before an expanded addressing method as described in Revision 3a of the ATA-6 Standard can be used. used.

327. Because the combination of Toombs and Revision 3a of ATA-6 discloses or suggests each and every element of claim 25, such combination renders obvious claim 25.

F. Toombs in View of ATA-6 Renders Obvious Claim 26

328. Claim 26 of the '486 Patent recites "[a] memory card according to claim 6, further comprising a register for storing the addressing data." This claim is obvious over Toombs in view of Revision 3a of the ATA-6 Standard.

329. As described above Revision 3a of the ATA-6 Standard describes a data register that stores addressing data indicative of an expanded or basic addressing method. Ex. 1008 at 63. Bit 10 of word 83, addressing data, is stored in the data register to be read by the host. Ex. 1008 at 22-23, 117. Revision 3a of the ATA-6 Standard therefore describes a register for storing the addressing data.

330. Because the combination of Toombs and Revision 3a of the ATA-6 Standard discloses or suggests each and every element of claim 26, such combination renders obvious claim 26.

G. Toombs in View of ATA-6 Renders Obvious Claim 27

331. Claim 27 of the '486 Patent recites "[a] memory card according to claim 26, wherein the stored addressing data comprises one bit." This claim is obvious over Toombs in view of Revision 3a of the ATA-6 Standard.

332. Revision 3a of the ATA-6 Standard describes a data register that stores addressing data indicative of an expanded or basic addressing method. Bit 10 of word 83, addressing data, is stored in the data register to be read by the

host. Ex. 1008 at 22, 117. Revision 3a of the ATA-6 Standard therefore describes addressing data comprising one bit stored to a register.

333. Because the combination of Toombs and Revision 3a of the ATA-6 Standard discloses or suggests each and every element of claim 27, such combination renders obvious claim 27.

H. Motivation to Combine Toombs and Revision 3a of the ATA-6 Standard

334. A POSITA would have been motivated to combine Toombs with the teachings of Revision 3a of the ATA-6 Standard to achieve a memory card capable of expanded addressing. A POSITA would have recognized that the memory card described in Toombs could not address more than 2GB of data, and would have been motivated to consider how the other leading mass storage standards had solved this problem when they reached the limits of the addressing methods inherent in their design. The prior-art in mass storage devices, such as disk drives in the case of Revision 3a of the ATA-6 Standard, encountered the same problem as Toombs of limited capacity. *Id*. Therefore there was a known need for the capability to access a larger number of addresses than the original standards allowed.

335. In Revision 3a of the ATA-6 Standard, the standard was expanded by increasing the number of address bits so that a larger number of addresses could be accessed. In order for a host to know whether a particular card

used the expanded addressing method, or only worked with limited addressing of the original standard, a bit was stored in the device so that the host could read that bit and, based on that bit, the host could know that it should use the expanded addressing method.

336. Further, a POSITA would understand that modifying Toombs with the teaching of Revision 3a of the ATA-6 Standard would enable a memory system to be able to calculate the capacity of the card based on a stored parameter such as C_SIZE. It would have been obvious to a POSITA to continue to use a parameter such as C_SIZE, and to expand the number of bits of the parameter to accommodate a larger capacity.

XIII. Reservation of Rights

337. My opinions are based upon the information that I have considered to date. I am unaware of any evidence of secondary considerations with respect to the '486 Patent that would render any of the asserted claims non-obvious. I reserve the right, however, to supplement my opinions in the future to respond to any arguments raised by the owner of the '486 Patent and to take into account new information that becomes available to me.

XIV. Conclusion

338. For the reasons given above, claims 6, 8-11, 22, 23, and 25-27 of the '486 Patent are unpatentable.

339. I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By: R. J. Baker MARCH 20, 2017
R. Jacob Baker, Ph.D., P.E.

APPENDIX A

R. JACOB BAKER, PH.D., P.E.

Professor of Electrical and Computer Engineering
Department of Electrical and Computer Engineering

6775 Agave Azul Court
Las Vegas, NV 89120

(725) 777-3755

Email: rjacobbaker@gmail.com
Website: http://CMOSedu.com/jbaker/jbaker.htm

EDUCATION

Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*

M.S. and B.S. in Electrical Engineering: May 1986 and 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

ACADEMIC EXPERIENCE

January 1991 - Present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, and the AFRL.
- Current research and development interests are:
  - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
  - Design of electrical/biological circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g. FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems
  - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces

- The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide)
- Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor
- Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
- Power electronics circuit design for consumers and consumer electronics

- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

INDUSTRIAL EXPERIENCE

2013 - present: Working with Freedom Photonics and Attollo Engineering in the Santa Barbara area on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits.

2013 - present: Working with National Security Technologies, LLC,) on the Design and Fabrication of Integrated electrical/photonic application specific integrated circuit (ASIC) design.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors with memory for very high-speed consumer imager products.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (now Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs (design is currently used in Micron's DDR memory), PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous projects (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1998: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and a graphics controller chip.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments. This position provided considerable fundamental grounding in EE with a broad exposure to PC board design to the design of cable equalizers. Also gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), krytrons, power MOSFETs, microwave techniques, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013 - 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015

- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Masters graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-present) for the *IEEE Solid-State Circuits Magazine*,.

ARMED FORCES

6 years United States Marine Corps reserves (Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge, October 23, 1987. Military Occupational Specialty was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Third Edition" *Wiley-IEEE*, 1174 pages. ISBN 978-0470881323 (2010) **Over 50,000 copies of this book's three editions in print.**

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Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICySSS keynote, IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING (last 5 years only)

Recent funding listed below. In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, $299,605
- Baker, R. J., (2017-2019) "High-Efficiency Integrated Si APD Quantum Key Receiver," Defense MicroElectronics Activity (DMEA), $266,029
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, $299,665
- Baker, R. Jacob, (2016-2017) "Testing and development of BiCMOS photodetectors and diagnostic instrumentation," Department of Energy, National Security Technologies, LLC, $181,605

- Baker, R. Jacob, (2016-2017) "Dual-Mode, Extended Near Infrared, Focal Plane Arrays fabricated with a Commercial SiGe BiCMOS Process," DARPA, $41,892
- Baker, R. Jacob, (2015-2016) "Photodetectors and high-speed electronics using Silicon Germanium (SiGe) Bipolar/CMOS (BiCMOS) integrated circuits," Department of Energy, National Security Technologies, LLC, $100,000
- Baker, R. Jacob, (2015-2016) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, $45,000
- Baker, R. Jacob, (2015) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), $45,000
- Baker, R. Jacob, (2014-2015) "NSTec ASIC Integrated Circuit Collaboration," Department of Energy, National Security Technologies, LLC, $90,000
- Baker, R. Jacob, (2014-2015) "Silicon Photonic-Electronic System Level Integration," U.S. Air Force/DOD, $54,607
- Baker, R. Jacob, (2013-2014) "NSTec ASIC Integrated Circuit Collaboration," Department of Energy, National Security Technologies, LLC, $162,074
- Baker, R. Jacob, (2013) "Design Software Setup," Department of Energy, National Security Technologies, LLC, $10,999
- Campbell, K. A. and Baker, R. J., (2009-2012) "Reconfigurable Electronics and Non-Volatile Memory Research" funded by the Air Force Research Laboratory, $2,790,081
- Baker, R. Jacob, (2010-2012) "Dual Well Focal Plane Array (FPA) Sensor," U.S. Navy, $31,500

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140. Baker, R. J., "Comparators for delta-sigma modulators," **9,135,962**, September 15, 2015.
139. Baker, R. J., "Resistive memory element sensing using averaging," **9,081,042**, July 14, 2015.
138. Baker, R. J., "Digital Filters with Memory," **9,070,469**, June 30, 2015.
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136. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,878,274**, November 4, 2014.
135. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,854,899**, October 7, 2014.
134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.
132. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,717,220**, May 6, 2014.
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71. Li, Y. and Baker, R. J., "A Highly Efficient and Reliable Electrowetting on Dielectric Device for Point-of-Care Diagnostics," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.

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62. Li, Y., Chen, R., and Baker, R. J., "A Fast Fabricating Electro-wetting Platform to Implement Large Droplet Manipulation," *Proceedings of the IEEE 57th International Midwest Symposium on Circuits and Systems*, pp. 326-329, August 3-6, 2014.
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15. Hartman, J. A., Baker, R. J., Gribb, M., Hill, H. H., Jessing, J., Moll, A. J., Prouty, and Russell, D., *A Miniaturized Ion Mobility Spectrometer (IMS) Sensor for Wireless Operation*, FAME (Frontiers in Assessment Methods for the Environment) Symposium, Sponsored by NSF, Minneapolis, Minnesota, August 10-13, 2003.
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10. Baker, R. J., "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society* Meeting, Boise, Idaho October 25, 2002.
9. Rivera, B., Baker, R. J., Melngailis, J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
8. Hess, H. and Baker, R. J., "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference* 2000, Boston, Massachusetts, September 2000.
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6. Baker, R. J., "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
5. Chen, H. and Baker, R. J., "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems," August 9-12, 1998.*
4. Liu, S. and Baker, R. J., "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems," August 9-12, 1998.*
3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40th International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers,* April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services are listed below. I have been deposed 23 times and given testimony at 3 trials.

Baker Botts LLP (Austin, TX, Dallas, TX, and Palo Alto, CA)

Case – *SanDisk LLC* v. Memory Technologies, LLC
Case Number - IPR2017-01022. Petition filed on March 3, 2017.
Case Number - IPR2017-00868. Petition filed on February 9, 2017.
Case Subject Matter – Memory cards including PC cards, compact flash ("CF") cards, secure digital ("SD") cards, and multimedia cards ("MMC")
Work Performed – Provided expert consulting services for inter partes review and wrote declaration.

Kilpatrick Townsend & Stockton LLP (Denver, CO and Shanghai, China)

Case – *Broadcom, Ltd.* v. Invensas
Case Number - IPR2017-00171. Petition filed on October 31, 2016.
Case Subject Matter – Semiconductor random access memory circuit timing and operation.
Work Performed – Provided expert consulting services and wrote declaration.

Paul Hastings LLP (Washington, DC)

Case – *Samsung, Inc.* v. ProMOS Technologies, Inc.
Case Numbers - IPR2017-00036, IPR2017-00038, and IPR2017-00039. Petitions filed on October 7, 2016.
Case Subject Matter – Sensing in semiconductor memory.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Munck Wilson Mandala LLP (Dallas, TX)

Case – *ams AG*, *ams-TAOS*, and *Samsung* v. JJL Technologies and 511 Innovations, Inc.
Case Numbers – IPR2016-01788, IPR2016-01792, IPR2016-01793, IPR2016-01804, IPR2016-01810, IPR2016-01818, and IPR2016-01819. Petitions filed on September 14, 2016.
Case Number - IPR2016-01787. Petition filed on September 13, 2016.
Case Subject Matter – Color and optical measuring systems.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C. (Boston, MA)

Case – *Netlist, Inc.* v. SK hynix
Case Number – ITC Investigation No. 337-TA-1023. Complaint filed on September 1, 2016.
Case Subject Matter – Memory modules and components and products containing same.
Work Performed – Provided expert consulting services including validity analysis and expert report.

Baker & Hostetler LLP (Cleveland, OH)

Case - *Evolv, LLC* v. Joyetech and Wismec
Case Number - California, CD 8:16-cv-00459.
Complaint filed on March 9, 2016. Case Subject Matter - Electronic personal vaporizers (also known as electronic cigarettes).
Work Performed - Provided expert consulting services including lab testing and infringement analysis. Wrote declaration.

Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C. (Boston, MA)

Case – *Advanced Silicon Technologies LLC* v. BMW, Fujitsu, Harman, Honda, NVIDIA, Renesas, Texas Instruments, Toyota, Volkswagen, and Audi
Case Number – ITC Investigation No. 337-TA-984. Complaint filed on December 28, 2015.
Case Subject Matter – Computing or graphics systems, components thereof, and vehicles containing same.
Work Performed – Provided expert consulting services.

DLA Piper (East Palo Alto, CA, Chicago, IL, and Reston, VA)

Case – Lincoln Electric v. *ESAB, Inc.*
Case Number – Texas, ED (Marshall) 2:15-cv-01404. Complaint filed on December 15, 2015.
Case Subject Matter – Power electronics for welding equipment.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, expert reports, and was deposed twice.

Weil, Gotshal & Manges LLP (Houston, TX and Redwood Shores, CA)

Case – *Micron Technology, Inc.* v. Innovative Memory Systems LLC
Case Numbers – IPR2016-00320, IPR2016-00322, IPR2016-00325, IPR2016-00326, and IPR2016-00327. Petitions filed on December 14, 2015.
Case Subject Matter – Data conversion, semiconductor fabrication, flash memory, and semiconductor memory device operation/control.
Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed three times.

Munck Wilson Mandala LLP (Dallas, TX) and O'Melveny & Myers LLP (Los Angeles, CA)

Case – 511 Innovations, Inc. v. *Samsung, Huawei, ZTE,* and *ams-TAOS*
Case Number – Texas, ED (Marshall) 2:15-cv-01526. Complaint filed on September 14, 2015.
Case Subject Matter – Color and optical measuring systems.
Work Performed – Provided expert consulting, claim construction, wrote declaration, expert reports, and was deposed twice.

Davis Wright Tremaine LLP (San Francisco, CA and Seattle, WA) and Mayer Brown LLP (Washington, DC)

Case – 511 Innovations, Inc. v. *Microsoft and Avago*
Case Number – Texas, ED (Marshall) 2:15-cv-01525. Complaint filed on September 14, 2015.
Case Subject Matter – Color and optical measuring systems.
Work Performed – Provided expert consulting services.

Weil, Gotshal & Manges LLP (Houston, TX, Redwood Shores, CA, and Washington, DC)

Case – *Micron Technology, Inc.* v. Limestone Memory Systems LLC
Case Numbers – IPR2016-00093, IPR2016-00094, IPR2016-00095, IPR2016-00096, and IPR2016-00097. Petitions filed on October 27, 2015.
Case Subject Matter – Semiconductor memory.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

DLA Piper (East Palo Alto and Los Angeles, CA)
Case – *Apple, Inc.* v. Longitude Flash Memory Systems S.A.R.L.
Case Number – IPR2015-01933. Petition filed on September 21, 2015.
Case Numbers – IPR2015-01924 and IPR2015-01925. Petitions filed on September 17, 2015.
Case Numbers – IPR2015-01908 and IPR2015-01909. Petitions filed on September 14, 2015.
Case Subject Matter – Non-volatile semiconductor flash memory fabrication and design.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Paul Hastings LLP (New York City, NY and Washington, DC)
Case – *Samsung, Inc.* v. Elbrus International Limited
Case Numbers - IPR2015-01523 and IPR2015-01524. Petitions filed on June 26, 2015.
Case Subject Matter – High-speed, low-power data transfer.
Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Kilpatrick Townsend & Stockton LLP (Menlo Park and San Francisco, CA)
Case – Consultant for *SK hynix*, Inc. on matters relating to investigation of certain patents owned by Longitude Licensing Ltd.
Case Subject Matter – Semiconductor random access memory and communication interfaces.
Work Performed – Provided expert consulting services in 2015.

Ropes & Gray LLP (New York City, NY)
Case – *Samsung, Inc.* v. Imperium IP Holdings (Cayman), Ltd.
Case Number – IPR2015-01233. Petition filed on May 21, 2015.
Case Subject Matter – Data interface circuits that can be either a single-ended interface or a differential interface.
Work Performed – Provided expert consulting services, wrote declarations for inter partes review, and was twice deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)
Case – *Silergy Corporation* v. Monolithic Power Systems, Inc.
Case Numbers – IPR2015-00803 and IPR2015-00804. Petitions filed on February 24, 2015.
Case Subject Matter – Microelectronic packaging.
Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Weil, Gotshal & Manges LLP (Houston, TX, Redwood Shores, CA, and Washington, DC)
Case – Limestone Memory Systems LLC v. *Micron Technology, Inc.*
Case Number – California, CD 8:15-cv-00278. Complaint filed on February 17, 2015.
Case Subject Matter – Semiconductor memory.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, and invalidity analysis.

Jones Day LLP (San Diego, CA)
Case – *Micron Technology, Inc.* v. eDigital Corp.

Case Number - IPR2015-00519. Petition filed on December 31, 2014.
Case Subject Matter – Methods for memory management in non-volatile flash memories.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (Atlanta, GA and Washington, DC)

Case – *Micron Technology, Inc.* v. MLC Intellectual Properties and BTG USA/International Inc.
Case Number - IPR2015-00504. Petition filed on December 24, 2014.
Case Subject Matter – Multi-level non-volatile floating gate memory, e.g. EPROM, EEPROM, and flash technologies.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Weil, Gotshal & Manges LLP (Houston, TX and Redwood Shores, CA)

Case – Innovative Memory Systems LLC v. *Micron Technology, Inc.*
Case Number – Delaware, 1:14-cv-01480. Complaint filed on December 15, 2014.
Case Subject Matter – Data conversion, semiconductor fabrication, flash memory, and semiconductor memory device operation/control.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, and invalidity analysis.

Skadden, Arps, Slate, Meagher & Flom LLP & Affiliates (Palo Alto, CA)

Case – ALFRED T. GIULIANO, Chapter 7 Trustee of the Ritz Estate; CPM ELECTRONICS INC.; E.S.E. ELECTRONICS, INC. and MFLASH, INC., on Behalf of Themselves and All Others Similarly Situated v. *SanDisk Corp.*
Case Number – California, ND (Oakland) 4:10-cv-02787. Fourth amended complaint filed on September 24, 2014.
Case Subject Matter – Non-volatile semiconductor flash memory fabrication and design.
Work Performed – Provided expert consulting services.

DLA Piper (East Palo Alto and Los Angeles, CA)

Case – Longitude Licensing Ltd. and Longitude Flash Memory Systems S.A.R.L., v. *Apple, Inc.*
Case Number – California, ND 3:14-cv-04275. Complaint filed on September 23, 2014.
Case Subject Matter – Non-volatile semiconductor flash memory fabrication and design.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, and invalidity analysis.

Singularity LLP (Redwood Shores, CA)

Case – VIA Technologies, Inc. v. *ASUS Computer International, AUSTEK Computer, and ASMedia Technology, Inc.*
Case Number – California, ND (San Jose) 5:14-cv-03586. Complaint filed on August 7, 2014.
Case Subject Matter – USB 3.0 circuits.
Work Performed – Provided expert consulting services including: non-infringement, invalidity, and trade-secret analyses. Wrote expert reports and was deposed twice.

Paul Hastings LLP (New York City, NY and Washington, DC)

Case – Cascades Computer Innovation, LLC v. *Samsung Electronics Co., Ltd.*
Case Number - Illinois, ED 14-cv-05691. Complaint filed on July 24, 2014.
Case Subject Matter – DRAM memory data transfer.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)

Case – Monolithic Power Systems, Inc. v. *Silergy Corporation*

Case Number - California, ND 3:14-cv-01745. First amended complaint filed on July 7, 2014.
Case Subject Matter – Microelectronic packaging.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Ropes & Gray LLP (East Palo Alto, CA, New York City, NY, and Washington, DC)
Case – Macronix International Co., Ltd. v. *Spansion, Inc.*, *Aerohive Networks*, *Allied Telesis*, *Ciena*, *Delphi Automotive*, *Polycom*, *Ruckus Wireless*, *ShoreTel*, *Tellabs*, and *TiVo*
Case Number – ITC Investigation No. 337-TA-922. Complaint filed on June 27, 2014.
Case Subject Matter – Devices containing non-volatile memory and products containing the same.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, Markman tutorial, and expert report.

Ropes & Gray LLP (Boston, MA and New York City, NY)
Case – Imperium IP Holdings (Cayman), Ltd. v. *Samsung, Inc.*
Case Number – Texas, ED (Sherman) 4:14-cv-00371. Complaint filed on June 9, 2014.
Case Subject Matter – Data interface circuits that can be either a single-ended interface or a differential interface.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, expert reports, deposition, and testimony at the trial.

Quinn Emanuel Urquhart & Sullivan, LLP (San Francisco, CA and Washington, DC)
Case – Freescale Semiconductor, Inc. v. *MediaTek, Inc.*, et. al.
Case Number – ITC Investigation No. 337-TA-920. Amended complaint filed on May 27, 2014.
Case Subject Matter – Semiconductor integrated circuits and devices containing the same.
Work Performed – Provided expert consulting services.

DLA Piper (East Palo Alto and San Diego, CA)
Case – *GSI Technology, Inc.* v. Cypress Semiconductor Corporation
Case Number – IPR2014-00419. Petition filed on February 7, 2014.
Case Subject Matter – Semiconductor static random access memory (SRAM) circuit design.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Ropes & Gray LLP (Washington, DC)
Case – Macronix International Co., Ltd. v. *Spansion, Inc.*, et al.
Case Number – Virginia, ED 3:13-cv-00679. Complaint filed on November 20, 2013.
Case Subject Matter – Non-volatile semiconductor flash memory fabrication and design.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Cooley LLP (San Diego, CA)
Case – HSM Portfolio LLC and Technology Properties Limited LLC v. Fujitsu, AMD, *Qualcomm, Inc.*, Elpida, SK Hynix, Micron, ProMOS, SanDisk, Sony, ST Micro, Toshiba, ON, and Zoran
Case Number – Delaware, 1:11-cv-00770. Third amended complaint filed on June 28, 2013.
Case Subject Matter – Semiconductor sensing circuits.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

DLA Piper (East Palo Alto and San Diego, CA)
Case – Cypress Semiconductor Corporation v. *GSI Technology, Inc.*
Case Number – California, ND 3:13-cv-02013. Complaint filed on May 1, 2013.
Case Subject Matter – Semiconductor static random access memory (SRAM) circuit design.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, and invalidity analysis.

Montgomery McCracken Walker & Rhoads LLP (Philadelphia, PA)

Case – Simon Nicholas Richmond v. Winchance Solar Fujian Technology, *Target*, *Creative Industries*, et. al.

Case Number – New Jersey, 3:13-cv-01954. Amended complaint filed on March 27, 2013.

Case Subject Matter – Circuitry including solar cells, re-chargeable batteries, energy conversion for solar lighting.

Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

DLA Piper (East Palo Alto, CA)

Case – Intellectual Ventures I/II LLC v. *Toshiba, Inc.*

Case Number – Delaware, 1:13-cv-00453. Complaint filed on March 20, 2013.

Case Subject Matter – Semiconductor memory and interface circuits.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, expert report, was deposed, and testified at trial.

Alston & Bird, DLA Piper, Gibson Dunn, Katten, O'Melveny, Orrick, and WilmerHale (various locations in the USA)

Case – Freescale v. *Funai*, *CSR*, *Zoran*, *MediaTek*, *Vizio*, *Sanyo*, *TPF*, *Top Victory Electronics*, *Envision Peripherals*, *AmTRAN*, and *Marvell*

Case Number – Texas, WD 1:12-cv-00644. Amended complaint filed on January 14, 2013.

Case Subject Matter – Semiconductor circuitry for voltage regulators, bus terminations, packaging, and signal processing.

Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, and Markman tutorial.

Amin, Turocy & Watson LLP (San Jose and San Francisco, CA)

Case – *InvenSense, Inc.* v. Robert Bosch GmbH

Case Subject Matter – Microelectromechanical systems (MEMS) sensor design and manufacture.

Work Performed – Provided expert consulting services in 2013.

Morrison & Foerster LLP (Los Angeles, Palo Alto, and San Francisco, CA)

Case – STMicroelectronics, Inc. v. *InvenSense, Inc.*

Case Number – California, ND 3:12-cv-02475. Complaint filed on May 16, 2012.

Case Subject Matter – Microelectromechanical systems (MEMS) sensors including Gyroscopes and accelerometers.

Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Kilpatrick Townsend & Stockton LLP (Menlo Park and San Francisco, CA)

Case – Consultant for *SK hynix*, Inc. on matters relating to investigation of certain patents owned by Round Rock Research LLC

Case Subject Matter – Semiconductor random access memory.

Work Performed – Provided expert consulting services in 2012.

Keker & Van Nest LLP (San Francisco, CA)

Case – Round Rock Research LLC v. *SanDisk Corp.*

Case Number – Delaware, 1:12-cv-00569. Complaint filed on May 3, 2012.

Case Subject Matter – Semiconductor non-volatile flash memory.

Work Performed – Provided expert consulting including: invalidity analysis, non-infringement analysis, expert reports, and was deposed.

Perkins Coie LLP (San Diego, CA)

Case – *ASUS Computer International* v. Round Rock Research LLC

Case Number – California, ND 3:12-cv-02099. Complaint filed on April 26, 2012.
Case Subject Matter – Semiconductor memory and image sensors.
Work Performed – Provided expert consulting, claim construction, non-infringement analysis, invalidity analysis, expert reports, and was deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)
Case – Dr. Michael Jaffe' as insolvency administrator for Qimonda AG v. LSI, *Atmel Corp*, Cypress, MagnaChip, and ON Semiconductor
Case Number – California, ND 3:12-cv-03166 (San Francisco). Complaint filed on January 10, 2012.
Case Subject Matter – Semiconductor processing and manufacturing.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Useful Arts IP (Cupertino, CA)
Case – Tezzaron (formerly Tachyon Semiconductor) v. *Elm Technology Corporation*
Case Number – Patent Interference No. 105,859. Declared on December 1, 2011.
Case Subject Matter – Packaging of semiconductors and through semiconductor vias.
Work Performed – Patent interference, wrote declaration, and was deposed.

Morgan, Lewis & Bockius LLP (Palo Alto, CA)
Case – Nanya Technology Corporation v. *Elpida Memory, Inc. and Kingston Technology Company, Inc.*
Case Number – ITC Investigation No. 337-TA-821. Complaint filed on November 21, 2011.
Case Subject Matter – Semiconductor DRAM design and manufacture.
Work Performed – Provided expert consulting and reports on validity, infringement, and domestic industry. Also provided declarations and was deposed.

Morgan, Lewis & Bockius LLP (Washington, DC)
Case – *Elpida Memory, Inc.* v. Nanya Technology Corporation
Case Number – ITC Investigation No. 337-TA-819. Complaint filed on November 15, 2011.
Case Subject Matter – Semiconductor DRAM design, fabrication, and manufacture.
Work Performed – Provided expert consulting and reports on infringement, domestic industry, and validity. Also provided Markman tutorial, declarations, deposition, and testimony at the trial.

Ropes & Gray LLP (New York City, NY)
Case – Intellectual Ventures v. *Sendai Nikon Corporation*
Case Number – Delaware, 1:11-cv-01025. Complaint filed on October 26. 2011.
Case Subject Matter – Image sensor design and manufacture.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Farella Braun + Martel LLP (San Francisco, CA)
Case – Round Rock Research LLC v. *Dell, Inc.*
Case Number – Delaware, 1:11-cv-00976. Complaint filed on October 14, 2011.
Case Subject Matter – Semiconductor DRAM design and manufacture.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Latham & Watkins LLP (San Francisco, CA)
Case – Altera Corp. v. *LSI Corp. and Agere Systems, Inc.*
Case Number – California, ND 4:11-cv-03139. Complaint filed on June 24, 2011.
Case Subject Matter – Semiconductor devices including phase-locked loops and clock recovery circuits.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Fish & Richardson P.C. (Washington, DC)

Case – Spansion LLC v. *Samsung Electronics Co., Ltd.*, Apple, Inc., Nokia Corp., PNY Technologies, Inc. Research In Motion Corporation, Transcend Information Inc.
Case Number – ITC Investigation No. 337-TA-735. Complaint filed on August 6, 2010.
Case Subject Matter – Semiconductor flash memory manufacture and design.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Jones Day LLP (Palo Alto, CA)

Case – LSI and Agere, Inc. v. *Xilinx, Inc.*
Case Number – New York, SD 1:09-cv-09719. Complaint filed on November 23, 2009.
Case Subject Matter – Semiconductor digital design and clocking.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Morrison & Foerster LLP (New York City, NY)

Case – Innurvation, Inc. et al v. *Fujitsu Microelectronics America, Inc.*, Sony Corporation of America, Toshiba America Electronics Components, Inc., and Freescale Semiconductor, Inc.
Case Number – Maryland, 1:09-cv-01416. Complaint filed on May 29, 2009.
Case Subject Matter – Semiconductor circuit layout.
Work Performed – Provided expert consulting, non-infringement analysis, and invalidity analysis.

Wilson Sonsini Goodrich & Rosati P.C. (Palo Alto, CA)

Case – Panavision Imaging, LLC, v. *OmniVision Technologies, Inc.*, Canon U.S.A., Inc., Micron Technology, Inc., Aptina Imaging Corporation, and Aptina, LLC.
Case Number – California, CD 2:09-cv-01577. Complaint filed on March 6, 2009.
Case Subject Matter – CMOS image sensor design and manufacture.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and wrote declaration.

McDermott Will & Emery (Menlo Park, CA)

Case – Volterra Semiconductor Corp. v. Primarion & *Infineon Technologies North America & Infineon Technologies, A.G.*
Case Number – California, ND 3:08-cv-05129. Complaint filed on November 12, 2008.
Case Subject Matter – High-performance analog and mixed-signal power management semiconductors.
Work Performed – Provided expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and was deposed.

pre-2008 Miscellaneous minor expert witness work, was deposed twice.

APPENDIX B

LIST OF EXHIBITS

1001	United States Patent No. RE45,486 (the "'486 Patent")
1002	File History for U.S. Patent No. RE45,486
1003	United States Patent No. 7,257,669 (the "'669 Patent")
1004	File History for United States Patent No. 7,257,669
1005	United States Patent No. 6,279,114 to Toombs et al.
1006	United States Patent No. 6,314,504 to Dent
1007	PC Card Standard, Volume 2 Electrical Specification
1008	The AT Attachment with Packet Interface - 6 Standard, Revision 3a
1009	Declaration of Dr. R. Jacob Baker
1010	The MultiMediaCard System Specification, Version 1.4 ("MMC Specification")
1011	United States Patent No. 6,260,101 to Hanzen
1012	Structured Computer Organization, Fourth Edition, by Andrew S. Tannenbaum
1013	United States Patent No. 6,253,300 to Lawrence et al.
1014	United States Patent Publication No. 2003/0235408 to Silvester et al.
1015	Affidavit of Christopher Butler, Internet Archive