DECLARATION OF VIJAY MADISSETTI, PH.D.
TABLE OF CONTENTS

I. BACKGROUND AND QUALIFICATIONS ................................................ 3
II. MATERIALS CONSIDERED................................................................. 12
III. OVERVIEW AND LEGAL STANDARDS........................................... 12
IV. DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME............................................................. 16
V. PERSON OF ORDINARY SKILL IN THE ART..................................... 16
VI. CLAIM CONSTRUCTION .................................................................... 17
   A. “matrix display”....................................................................................... 18
   B. “multi-level” ............................................................................................ 19
   C. “multi-level timing controller”................................................................. 20
VII. PRIOR ART ........................................................................................ 23
   A. Ex. 1004 – U.S. Patent No. 6,320,590 to Yong-Suk Go (“Go”)............. 23
   B. Ex. 1005 – U.S. Patent No. 5,913,075 to Beers et al. (“Beers”)......... 25
   C. Ex. 1006 – U.S. Patent No. 5,900,857 to Kuwata et al. (“Kuwata”) ..... 29
   D. Ex. 1007 – U.S. Patent No. 6,324,602 to Chen et al. (“Chen”) ............ 31
   E. Ex. 1001 – The ’247 Patent’s Admitted Prior Art (the “’247 APA”)........................................................................ 34
VIII. OPINIONS ABOUT THE ’247 PATENT ........................................ 35
   A. GROUND 1: Claims 1-10 are Obvious under 35 U.S.C. § 103(a) over Go in view of Beers (collectively, “Go-Beers”).............................. 35
   B. GROUND 2: Claims 1-10 are Obvious under 35 U.S.C. § 103(a) over Kuwata in view of Chen (collectively, “Kuwata-Chen”)............. 54
I, Vijay Madisetti, Ph.D., declare as follows:

I. BACKGROUND AND QUALIFICATIONS

1. I have been retained by Greenberg Traurig, LLP, on behalf of Valens Semiconductor Ltd. (“Valens”), as an expert in the above-captioned proceeding. I have been asked to render an opinion regarding the validity of claims 1-10 (“Challenged Claims”) of U.S. Patent No. 6,611,247 (“the ’247 Patent”; Ex. 1001). I am being compensated at a rate of $670.00 per hour for my study and testimony in this matter. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

2. I submit this declaration based on my personal knowledge and in support of Valens’ inter partes review petition (“Petition”) regarding the ’247 Patent.

3. I am a tenured Professor in Electrical and Computer Engineering at the Georgia Institute of Technology (“Georgia Tech”). I have worked within the area of embedded computing systems, wireless communications, and digital signal processing for over twenty-five years, and have authored, co-authored, or edited several books and numerous peer-reviewed technical papers in these areas.

4. I received my B. Tech (Hons) in ECE from the Indian Institute of Technology (IIT), Kharagpur, India in 1984. I obtained my Ph.D. in Electrical
Engineering and Computer Science at the University of California, Berkeley, in 1989. I received the Demetri Angelakos Outstanding Graduate Student Award from the University of California, Berkeley and the IEEE/ACM Ira M. Kay Memorial Paper Prize in 1989.

5. I joined Georgia Tech in Fall of 1989 and am now a tenured Professor in Electrical and Computer Engineering. I have been active in the areas of computer systems, embedded systems, multimedia (audio, video, speech, wireless, etc.), wireless communications, digital signal processing, integrated circuit design (analog & digital), software engineering, system-level design methodologies and tools, and software systems. I have been the principal investigator (“PI”) or co-PI in several active research programs in these areas, including DARPA's Rapid Prototyping of Application Specific Signal Processors, the State of Georgia's Yamacraw Initiative, the United States Army's Federated Sensors Laboratory Program, and the United States Air Force Electronics Parts Obsolescence Initiative. I have received an IBM Faculty Award and NSF's Research Initiation Award. I have been awarded the 2006 Frederick Emmons Terman Medal by the American Society of Engineering Education for contributions to Electrical Engineering, including authoring a widely used textbook in the design of VLSI digital signal processors.

6. I have created and taught undergraduate and graduate courses in
hardware and software design for computer systems, control systems, signal processing and wireless communication circuits at Georgia Tech for the past twenty years.

7. I have been an active consultant to the automotive and electronics industries and various research laboratories (including Massachusetts Institute of Technology Lincoln Labs and Johns Hopkins University Applied Physics Laboratory (“APL”)). I have founded three companies in the areas of computing systems & processors, buses, and embedded avionics and wireless software, military chipsets involving imaging technology and guidance technologies, and wireless communications. I have supervised the Ph.D. dissertations of over twenty engineers in the areas of computer engineering, signal processing, communications, rapid prototyping, and system-level design methodology, of which five have resulted in thesis prizes or paper awards.

8. My consulting work for MIT Lincoln Labs involved high resolution imaging for defense avionics applications, where I worked in the area of prototyping complex and specialized computing systems. My consulting work for the APL mainly involved localization of objects in image fields, where I worked on identifying targets in video and other sensor fields and identifying avionics computer architectures and circuits for power and space-efficient designs.

9. I have developed wireless baseband and protocol stack software and
assembly code for a leading telecommunications handset vendor that focused on efficient realization of speech codecs and echo-cancellation. My work in this regard included creation of software code, and analysis and revision of existing software code. This work spanned approximately three years of industry work between 2000 and 2004.

10. The first of the companies I founded, VP Technologies, offers products in the area of semiconductor integrated circuits, including building computing systems for advanced display & imaging systems in United States Air Force helicopters. I remain a director of VP Technologies. The second of these companies, Soft Networks, LLC, offers software for multimedia and wireless computing platforms, including the development of a set-top box for Intel that decodes MPEG-2 video streams and imaging codes for multimedia phones. The technology involved with the design, development, and implementation of the Intel set-top box included parsing the bit streams, decoding communications protocols, extracting image and video data, and then processing for subsequent display or storage. The third of these companies, Elastic Video, uses region of interest based video encoding or decoding for capturing high quality video at very low bit rates, with primary application for wireless video systems.

11. I have been elected a Fellow of the IEEE, for contributions to embedded computing systems. The Fellow is the highest grade of membership of
the IEEE, a world professional body consisting of over 300,000 electrical and electronics engineers, with only one-tenth of one percent (0.1%) of the IEEE membership being elected to the Fellow grade each year. Election to Fellow is based upon votes cast by existing Fellows in IEEE.


13. I have designed several specialized computer and communication systems over the past two decades at Georgia Tech for tasks such as wireless audio and video processing and protocol processing for portable platforms, such as cell phones and PDAs. I have worked on designing systems that are efficient from performance, size, weight, area, and thermal considerations. I have developed courses and classes for the industry on these topics, and many of my lectures in advanced computer system design, developed under the sponsorship of the United
States Department of Defense in the late 1990s, are available for educational use at “http://www.eda.org/rassp“ and have been used by several U.S. and international universities as part of their course work. Some of my recent publications in the area of design of wireless communications systems and associated protocols are listed in Appendix A, my CV.

14. I am knowledgeable and familiar with standards related to the automotive, avionics, wireless and telecommunications systems industries, and as shown in Appendix A, some of my papers describe the application of these standards in optimizing the design and testing of these systems. I am also knowledgeable and familiar with microprocessor architecture and associated software and firmware design for embedded, wireless and telecommunications terminals and base stations.

15. I have authored, co-authored, or edited several books in the area of computer systems and distributed systems in the past twenty years, including:

- VLSI Digital Signal Processors, *Madisetti, V.K.*
- Quick-Turnaround ASIC Design in VHDL, Romdhane, M., Madisetti, V.K., Hines, J.
- VHDL: Electronics Systems Design Methodologies, *Madisetti, V.*
K. (Editor)

- Platform-Centric Approach to System-on-Chip (SoC) Design, Madisetti, V. K., Arpnikanondt, A.

16. In the past decade I have also authored several peer-reviewed papers in the area of computers, computer software applications, and software design, and these include:


17. In the late 2000s, I collaborated with a leading automotive supplier to design and development embedded software and electronic control unit (“ECU”) controller modules in the area of energy profiling for hybrid/gas cars (described in U.S. Provisional Patent App. No. 61/209,403). The system we developed is described in more detail in the figures below:
18. I have designed and implemented multiple processor computing systems that perform multimedia tasks (e.g., speech and audio recognition) and also avionics/embedded guidance systems since the mid-1990s, and I have also implemented real-time operating systems in the same time frame. Representative publications of my work in these areas include, *The Georgia Tech Digital Signal Multiprocessor* (DSMP), IEEE Transactions on Signal Processing, Vol 41, Issue 7, 1993, and “*Task Scheduling on the Georgia Tech Digital Signal Multiprocessor*”, Proc. IEEE ICASSP 1992. More recent work that is related to multimedia processing on multiprocessor systems can be found in “*A Dynamic Resource Management and Scheduling Environment for Embedded Multimedia and Communications Platforms*”, IEEE Embedded Systems Letters, Vol 3, Issue 1, 2011. Three generations of Digital Signal Multiprocessors (DSMP’s) (listed in the table below) were designed at Georgia Tech as part of my research and education efforts.

19. In collaboration with the US Air Force, Lockheed Martin, and Hughes Corporation, I designed and implemented a 192-processor multiprocessor system utilizing a number of buses and crossbar switches for processing real-time avionics data (infrared search and track applications – IRST), and this represented one of the largest multiprocessor systems used in the mid-1990s timeframe on aircraft. See my publications, “*Virtual Prototyping of Embedded Microcontroller-Based*
Based on the above education and experience, I believe that I have a detailed understanding of the state of the art during the relevant period, as well as a sound basis for opining how persons of skill in the art at that time would understand the technical issues in this case.

A copy of my curriculum vitae is attached hereto as Appendix A.

II. MATERIALS CONSIDERED

The analysis provided in this Declaration is based on my education as well as my experience in the field. In addition to relying upon my knowledge based on written materials and other information that was known prior to the effective filing date of the ’247 Patent, which I have been told is the July 1, 1999, I have considered the materials attached as Appendix B.

III. OVERVIEW AND LEGAL STANDARDS

I have been asked to provide opinions regarding the validity of claims of the ’247 Patent in light of several prior art patents and publications.

I understand that the following standards—which are taken from 35 U.S.C. § 102—govern the determination of whether a claim in a patent is invalid as “anticipated.”

In general, a patent claim is invalid as “anticipated” if each and every
feature of the claim is found, expressly or inherently, in a single item of prior art. In determining whether the single item of prior art anticipates the claim, one considers not only what is expressly disclosed in the particular item of prior art, but also what is inherently present or disclosed in that prior art or what inherently results from its practice. Claim limitations that are not expressly found in a prior art reference are inherent if the prior art necessarily functions in accordance with, or includes, the claim limitations, or if the missing element or feature would be the natural result of following what the prior art teaches to persons of ordinary skill in the art. It is acceptable to examine evidence outside the prior art reference (extrinsic evidence), including experimental testing, in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it. Mere probabilities are not enough, but it is not required that persons of ordinary skill actually recognized the inherent disclosure at the time the prior art was first known or used.

26. I understand that there are a number of different ways that anticipation can occur. First, if the claimed invention was “known or used by others” in this country before the asserted date of invention, then the claim is anticipated. A demonstration or oral presentation could suffice; printed publications are not required. Second, if the claimed invention was “in public use” in this country more than one year prior to the date of the application for the patent in the United States,
then the claim is anticipated. Public knowledge of the invention or an enabling disclosure is not required; only public use is required. Third, if the claimed invention was “described in a printed publication” anywhere in the world prior to the alleged invention or more than one year prior to the date of the application for the patent in the United States, then the claim is anticipated. To anticipate, however, the printed publication must also enable one skilled in the art to make and use the claimed invention. Fourth, if the claimed invention was made in this country by another inventor before the asserted date of invention, and not abandoned, suppressed, or concealed, then the claim is anticipated. It is normally the first inventor to conceive, rather than the first to reduce to practice, who is entitled to priority, assuming that the first to conceive was reasonably diligent in reducing the invention to practice from a time prior to conception by the other.

27. It is also my understanding that a claimed invention is unpatentable under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the alleged invention was made to a POSITA. This is sometimes described as “obviousness.” I understand that an obviousness analysis takes into account the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter.

28. It is my understanding that the Supreme Court, in *KSR Int’l Co. v.*
Teleflex Inc., 550 U.S. 398 (2007) and other cases, has recognized several rationales for combining references or modifying a reference to show obviousness of the claimed subject matter. Some of these rationales include the following: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art or combine prior art teachings to arrive at the claimed invention. I also understand that a POSITA is a person of ordinary ingenuity and creativity, not an automaton.

29. It is my understanding that when a patent simply arranges old elements with each performing the same function it would have been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious.

30. It is my understanding that a preamble generally does not limit a claim. I understand that a preamble is not limiting when a claim is structurally complete invention in the claim body and the preamble only states a purpose or intended use for the claimed invention.
IV. DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME

31. I have carefully reviewed the specification, drawings, and claims of the ’247 Patent.

32. Based on my review of these materials, and the materials listed in Appendix B, I believe that the relevant field for purposes of the ’247 Patent is data transfer systems for integrated circuits:

“FIELD OF THE INVENTION

The present invention relates to a matrix display system, and more particularly, to a display data transfer system and method for a matrix display in which multi-level signaling is used for transferring display data needed for image display on a display panel.

(Ex. 1001 at 1:7-11).

I have been informed that the relevant timeframe runs up to July 1, 1999.

33. As described above and in my C.V., I have extensive experience in the relevant technical field. Based on my experience and expertise in this field, I have an understanding of the relevant field in the relevant timeframe.

V. PERSON OF ORDINARY SKILL IN THE ART

34. To assess the level of ordinary skill in the art of the ’247 Patent, I have considered the type of problems encountered in the art, the prior solutions to those problems found in prior art references, the rapidity with which innovations are made, the sophistication of the technology, the level of education of active
workers in the field, and my own experience working with those of skill in the art at the time of inventions. In my opinion a person of ordinary skill ("POSITA") in the art of the '247 Patent at the time of the effective filing date (July 1, 1999) would have at least a Bachelor’s degree in Electrical Engineering, Computer Engineering or the equivalent, and either 2-3 years of relevant experience relating to circuits for computers and computer subsystems, or alternatively, an advanced degree in Electrical Engineering, Computer Engineering or the equivalent.

VI. CLAIM CONSTRUCTION

35. I understand that a claim subject to *inter partes* review must be given its broadest reasonable construction that is consistent with the specification of the patent.

36. I understand that the meaning of a claim term is a meaning that the term would have to a POSITA at the time of the invention. I also understand that I am to consider a claim term in the context of the entire patent, including the specification in determining the meaning to a POSITA. I further understand that, under the doctrine of claim differentiation, the presence of a dependent claim that adds a limitation creates a presumption that the independent claim it depends from does not require this limitation.

37. I have been asked to provide my opinion with respect to three claim terms from the ’247 Patent ("matrix display,” “multi-level” and “multi-level timing
controller”), which I provide below. In my opinion, the broadest reasonable construction of the remaining terms in the Challenged Claims is consistent with their plain meaning as understood by a POSITA, and no further construction is necessary.

A. **“matrix display”**

38. In my opinion, the broadest reasonable construction of “matrix display” is:

“a display that comprises a plurality of picture element circuits arranged as a matrix, such as a liquid crystal display (LCD).”

The ’247 Patent does not expressly define the term “matrix display.” However, the above construction is consistent with a POSITA’s understanding of the term in light of the specification, which makes clear that the term “matrix display” is to be used interchangeably with “LCD.” For example, the Field of the Invention section of the ’247 Patent states that the “present invention relates to a matrix display system” and further states that this “description is made with reference to a liquid crystal display (LCD)”:

The present invention relates to a matrix display system, and more particularly, to a display data transfer system and method for a matrix display in which multi-level signaling is used for transferring display data needed for image display on a display panel.
Hereinafter, the description is made with reference to a liquid crystal display (LCD).

(Ex. 1001 at 1:6-13). Further, in describing the background of the invention, the ’247 Patent explains that “liquid crystal displays, electro-luminescence displays and electro chromic (EC) displays ... [g]enerally ... comprise[] a plurality of picture element circuits arranged as a matrix.” (Id. at 1:19-23). According, a “matrix display” is “a display that comprises a plurality of picture element circuits arranged as a matrix, such as a liquid crystal display (LCD).”

B. “multi-level”

39. In my opinion, the broadest reasonable construction of “multi-level” is:

“having three or more meaningful levels”

As a preliminary matter, the ’247 Patent does not expressly define the term “multi-level.” However, in order to overcome 35 U.S.C. § 112, First Paragraph rejections during prosecution, the applicant of the ’247 Patent (“Applicant”) admitted that “multilevel digital signals and multilevel transmission are well understood by those of ordinary skill in the art” and provided a dictionary definition for “multilevel transmission” to illustrate this. (Ex. 1002 [’247 FH] at 95, 111, 145-46). Specifically, Applicant relied on the McGraw-Hill Dictionary of
Scientific and Technical Terms (4\textsuperscript{th} Ed., 1989), which defines “multilevel transmission” as “transmission of digital information in which three or more levels of voltage are recognized as meaningful, as 0, 1, 2 instead of simply 0, 1.” (Ex. 1002 [’247 FH] at 145-46). I agree that the definition that Applicant relied upon to overcome the Section 112 rejections (\textit{id.}) supports the broadest reasonable construction. Thus, it is my opinion that “multi-level” means “having three or more meaningful levels.”

\textbf{C. \textit{“multi-level timing controller”}}

40. In my opinion, the broadest reasonable construction of “multi-level timing controller” is:

“a controller for converting digital data to a clocked multi-level signal for transferring over a bus.”

This construction is consistent with the claim language and a POSITA’s understanding of the term in light of the specification. As a preliminary matter, it is my opinion that a POSITA would understand that a timing controller, by its very name, is a controller for transferring “clocked” signals (i.e. signals transmitted in relation to a clock). Further, independent claims 1, 3 and 6 each define materially similar functions for how the “\textit{multi-level} timing controller” operates. For example, Claims 1 and 6 each require “a multi-level timing controller for receiving a digital data input and converting it into a multi-level signal display data output.”
Claim 3 similarly requires the step of “converting a first digital data signal into a multi-level signal display data output by a multi-level timing controller.” Accordingly, a multi-level timing controller must be capable of converting digital data into a multi-level signal.

41. This construction is consistent with the embodiments disclosed in the specification. For example, Figure 7 of the ’247 Patent is “a schematic view of a multi-level timing controller according to the present invention.” (See Ex. 1001 at 3:23-24). As shown below in Figure 7 and explained in Column 4, N bits of digital data input are converted by the multi-level timing controller 70 into N/\log_2 L lines of multi-level data output, where L is the number of levels that may be encoded in the multi-level signal:

(Id. at Fig. 7, 4:19-25, 4:42-61).

42. Specifically, the ’247 Patent states:

According to the present invention, as shown in FIG. 7, in addition to a timing generator 72, a multi-level timing controller 70 further
comprises a multi-level encoder 74 in which an N-bit digital data input is encoded into a multi-level (L-level) data output by the multi-level encoder 74, and N/ log₂L data lines are needed for output.

(Id. at 4:19-25 (emphasis added)). In the Figure 7 embodiment, the process of converting digital data to a multi-level signal is performed by the multi-level encoder. I understand that, under the doctrine of claim differentiation, since Claim 1 requires a “multi-level timing controller” and Claim 2 requires that the “multi-level timing controller” comprise “a multi-level encoder,” the construction of a “multi-level timing controller” cannot be limited to a specific embodiment of the “multi-level timing controller” where the function of “converting digital data to a … multi-level signal” is performed by a multi-level encoder.

43. Table 4 of the ’247 Patent and the portions of the specification relating to Table 4 confirm the clocked nature of the multi-level signal. (See Ex. 1001 ['247 Patent] at 5:23-48). For example, the ’247 Patent explains that “[w]hen the data input speed of the timing controller is 1 pixel/clock and the output speed is 2 pixels/clock, the operation frequency can be halved according to the present invention.” (Ex. 1001 ['247 Patent] at 5:42-44). Thus, it is my opinion that a POSITA would understand that the timing controller of the present invention (i.e. a multi-level timing controller) outputs a signal that is clocked. Further, as detailed above, the “multi-level timing controller” also comprises a “timing generator” in
the Figure 7 embodiment.

44. Accordingly, it is my opinion that a POSITA would understand that the claim term, “multi-level timing controller,” means “a controller for converting digital data to a clocked multi-level signal for transferring over a bus.”

VII. PRIOR ART

A. Ex. 1004 – U.S. Patent No. 6,320,590 to Yong-Suk Go (“Go”)

45. Go teaches the use of a “bus compression apparatus for compressing data … to suppress an EMI signal and to simplify a data bus.” (Ex. 1004 at Abstract). Specifically, Go teaches the use of a bus compressor and a corresponding bus decompressor to transmit video data from a computer system’s video card to an LCD. (Id. at 3:12-14, 3:29:43). Figure 7 of Go, shown below, is a schematic view of an LCD computer system employing the above invention, the material components of which are highlighted as follows:

- Bus compressor 34 (blue)
- FPC cable 36 (yellow)
- Bus decompressor 46 (pink)
- Liquid crystal panel 42 (green)
Go teaches the use of a multi-level encoder (i.e. bus compressor 34) which “compresses the 18-bit video data VD from the first data bus 31 to 9-analog signals” (i.e. 9 multi-level signals) and transmits the analog signals over FPC cable 36. (See Ex. 1004 at 3:50-51; 3:58-62). Go further teaches the use of a multi-level decoder (i.e. bus decompressor 46) which “quantizes and codes the 9-analog signals AMS from the second connector 36B of the FPC cable 36 to substantially reconstruct 18-bit video data VD.” (See Ex. 1004 at 4:1-4). Go further teaches that the reconstructed video data VD “for one pixel line are distributively and
simultaneously inputted to each D-IC 44 the output of which are supplied to the
liquid crystal panel 42 to drive the pixels for one line.” (See Ex. 1004 at 4:16-19).

B. **Ex. 1005 – U.S. Patent No. 5,913,075 to Beers et al. (“Beers”)**

47. Beers teaches an architecture for “converting digital signals into
multilevel analog signals for current source based transmission over a bus, and
related reconversion to digital format at the receiving end of the bus.” (Ex. 1005 at
1:21-25). This includes a “system and method which uses accurately coded and
decoded analog currents to simultaneously transmit over a single line multiple
digital bits between separate integrated circuit devices, effectively extending the
line bandwidth.” (Ex. 1005 at 6:63-67). Specifically, Beers teaches an
architecture that receives “digital [format] signals at a first cycle rate, … latch[es]
the digital format signals for multiple successive cycles, … convert[s] latched
digital format signals into multilevel analog format signals, … send[s] the analog
format signals from a transmitting end of a bus to a receiving end of the bus, [and]
convert[s] analog format signals received from the bus into received digital format
signals distributed over multiple successive cycles.” (Ex. 1005 at 1:66 – 2:12).

48. A schematic diagram illustrating the use of this architecture to
transmit data between a processor and a peripheral device is shown below, the
material components of which are highlighted as follows:
- Interface Latches 6, Current Source Drivers 7, Reference Generator 8 (blue)
- I/O Bus 3 (yellow)
- Peripheral Mux 11, Multilevel Converter 12, Reference Replicator 13 (pink)
- Peripheral 2 (green)

(Id. at Fig. 2).

49. Beers teaches a “multi-level timing controller” for receiving a digital data input and converting it into a multi-level signal display data output. The “multi-level timing controller” comprises:
• interface latches 6
• a PROC CLK or processor clock
• an I/O CLK or I/O clock
• current source drivers 7
• reference generator 8

(See Ex. 1005 [Beers] at Fig. 2)]. The “multi-level timing controller” of Beers receives input at interface latches 6 based clock rate of PROC CLK or processor clock (Id. at Fig. 2, 5:57-66) and provides as an output digital bit pair A and B, which are clocked at the frequency set by the I/O clock. (Id. at Fig. 2, 5:57 – 6:7). Beers teaches the use of a multi-level encoder (i.e. current source drivers 7) which “uses the reference signal generated by reference generator 8 to perform the digital to analog conversion between digital bit pair A and B and analog output current \(i_T\).” (Id. at 4:51-54). Accordingly, Beers teaches a controller for converting digital data to a clocked multi-level signal for transferring over a bus (i.e. a multi-level timing controller).

50. Beers further teaches that the multi-level signal above, current \(i_T\), is transferred over a multi-level signal bus (i.e. I/O bus 3) and received by a multi-level input data driver, which comprises:

• peripheral mux 11
• an I/O CLK or I/O clock
- multi-level converter 12
- reference replicator 13

(Id. at Fig. 2]. Beers teaches that the “multi-level input data driver” of Beers receives the multi-level input signal transferred over I/O bus 3, current \( i_T \), at multi-level converter 12, which is a multi-level decoder. (Id. at Fig. 2, 4:59 – 5:11, Fig. 4; 6:18-53). Multi-level converter 12 converts the multi-level signal, current \( i_T \), into bits A and B (i.e. digital data). (Id. at Fig. 2, 4:59 – 5:11, Fig. 4; 6:18-53, Fig. 10). Ultimately, bits A and B are transferred to peripheral 2 through peripheral mux 11. (Id. at Fig. 2, 6:6-17, Fig. 9).

51. Beers teaches that a “problem typically arises in the context of computer systems in which the integrated circuit devices associated with the processor and the integrated circuit devices associated with the peripherals have a clock rate capability materially faster than the printed circuit board wiring inductance and capacitance constraints allow for the bus itself.” (Id. at 3:8-14 (emphasis added)). This problem is further explained in U.S. Patent No. 5,793,223 to Richard Francis Frankeny (“Frankeny”) [Ex. 1008], which Beers incorporates by reference. (Ex. 1005 at 1:7-14). Frankeny teaches that “[c]omputer system clock speeds continue to increase [and] the measurement of data signals subject to change at such high frequencies is becoming more difficult because of impedance mismatch induced reflections on the connecting lines.” (Ex. 1008 at 1:26-31
(emphasis added); see also id. at 1:31-45). It is my opinion that a POSITA would understand that these “impedance mismatch induced reflections” are a form of EMI. Frankeny teaches that these reflections (and thus, EMI) may be reduced by matching the impedance through the use of an active terminator circuit connected to a transmission line. (See Ex. 1008 at Abstract, 6:6-10, 2:59-64, 3:22-44, 4:32-37).

C. Ex. 1006 – U.S. Patent No. 5,900,857 to Kuwata et al. (“Kuwata”)

52. Kuwata teaches a driving circuit for transmitting video data to an LCD. Specifically, in the Background of the Invention, Kuwata teaches a prior art “driving circuit 200 for a liquid crystal display device” as illustrated in Figure 15, shown below. (Ex. 1006 [Kuwata] at 4:39-47).

(Ex. 1006 [Kuwata] at Fig. 15, 11:4-5). Kuwata states:
As shown in FIG. 15, respective picture image data of R, G and B having graduation information are inputted to a frame modulation circuit 110. ... A memory 130 consisting of VRAM stores picture image data corresponding to one frame. The memory 130 stores data in such a manner that the data of RGB are collected together in a set and each RGB data on an L number of simultaneously selected row electrodes which correspond to a column electrode are set to an L number of continuous addresses. Accordingly, when reading of data is conducted successively from the memory 130 according to an access mode, data corresponding to voltages applied to column drivers 80 are outputted. The data in the memory 130 are outputted to a format converter 190 in synchronism a timing of data input.

(Id. at 4:47-67).

53. Kuwata further states:
The column voltage signal generator 180 produces voltage values to be applied to column electrodes based on a row selection pattern from a row selection pattern generator 7 and the output of the format convertor 190. The row selection pattern from the row selection pattern generator 7 is supplied also to row drivers 90. The column drivers 80 and the row drivers 90 drive column electrodes and row
electrodes of a liquid crystal display pattern 40 based on the inputted signals. A driver control circuit 60 controls a driving timing to the column drivers 80 and the row drivers 90.”

(Id. at 5:4-16).

54. During the prosecution of the ’247 Patent, the Applicant argued that the claims were novel over Kuwata because Kuwata allegedly “fails to disclose any conversion of the input [display] signals into multi-level signals to be transferred on a multi-level bus and subsequent conversion of the multi-level signal to a data driving signal for a matrix display panel.” (Ex. 1002 ['247 FH] at 148-49 (Appeal Brief, March 10, 2003)).

D. Ex. 1007 – U.S. Patent No. 6,324,602 to Chen et al. (“Chen”)

55. Chen relates to advanced input/output interfaces for integrated devices such as memory devices. (Ex. 1007 [Chen] at 1:7-10, Abstract). It is my opinion that a POSITA would understand that the teachings of Chen would also apply to interfaces between graphics memories (e.g., frame buffers) and display controllers/drivers. (See Ex. 1007 at 2:55-67). A POSITA would further understand that Chen teaches solutions that overcome the deficiencies of the prior art when applied to “projected memory bandwidth requirement for multimedia three-dimensional graphics applications.” (Id.). Chen also teaches the problems with EMI, large chip area and power consumption requirements of existing
solutions and teaches solutions that substantially reduce or eliminate these problems with prior art interfaces. (Id. at 2:43-54).

Specifically, Chen teaches the use of an “advanced input/output interface allows for high speed/bandwidth memory accesses while reducing the pin count and operating frequency required for operation.” (Id. at Abstract). Chen further teaches that the “I/O interface may include at least one bit compression circuit (BCC) and at least one bit decompression circuit (BDC) to compress and decompress data/address/control signal information at the input/output pins of the memory device.” (Id. at 2:65 – 3:2). A diagram illustrating the use of this interface is shown below, the material components of which are highlighted as follows:

- Bit Compression Circuit (BCC) 24, PLL Clock Generator 31 (blue)
- Bus 22 (yellow)
- Bit Decompression Circuit (BDC) 38 (pink)
Chen states:

Control device 14 is connected to memory device 12 by memory bus 22. Control device 14 transfers data and other information to and from memory device 12 for control, addressing, processing, and other operations. Control device 14 can be an IC device, such as an application specific integrated circuit (ASIC), which can be incorporated into a host computer.”

(Id. at 7:37-43).
57. Chen further states that “BCC 24 generally functions to convert a plurality (i.e., n) of two-level protocol signals received over a respective bus 30 into a single, multi-level protocol signal which is output on a respective line 32.” (Id. at 8:19-23). Chen further states that, “[f]or a multi-level protocol signal output by the respective BCC 24, each VGC circuit 28 outputs a controlled signal which is placed on bus 22 connecting to control device 14.” (Id. at 7:12-17).

58. BDC 38 receives the multi-level protocol signal placed on bus 22 by the respective BCC 24. (Id. at Fig. 1). BDC 38 is “substantially similar” to BDC 26. (Id. at 7:6-17). “BDC 26 functions to convert a single multiplexed signal (D'k) formatted in a multi-level protocol and received over line 32 into a plurality of respective two-level protocol signals (D'k(0)-D'k(n−1)) which are then output on a respective bus 30.” (Id. at 9:26-30).

E. Ex. 1001 – The ’247 Patent’s Admitted Prior Art (the “’247 APA”)

59. The ’247 Patent states that “a prior art digital input data driver 20 shown in FIG. 4, data from FIG. 3 passes through an input data register 22, an internal processing logic 24 and a digital-to-analog converter (DAC) to become an analog signal output, which is a data driving signal.” (Ex. 1001 [’247 APA] at 4:28-32).

60. Further, in the Background of the Invention,” the ’247 Patent teaches that a “6-bit XGA notebook” with an LCD and a “data transfer system of the LCD”
was known prior art. (Id. at 2:19-20, 3:11-12, Fig. 2).

61. Further, in the Background of the Invention,” the ’247 Patent teaches that a “conventional active matrix LCD” would include “a plurality of scan bus lines Y1, Y2, …, Yn” and a scan driver 10 for driving said scan bus lines. (Id. at 1:27-40, Fig. 1).

VIII. OPINIONS ABOUT THE ’247 PATENT

62. My invalidity analysis is set forth in the following sections and my attached claim charts, Ex. 1009 and 1010.

63. I understand that the claims at issue, i.e. the Challenged Claims, are claims 1-10 of the ’247 Patent.

A. GROUND 1: Claims 1-10 are Obvious under 35 U.S.C. § 103(a) over Go in view of Beers (collectively, “Go-Beers”)

1. Challenged Claims

[CLAIM 1-PREAMBLE] A data transfer system for a multi-level signal for providing a display data to a matrix display panel, comprising:

64. It is my opinion that a POSITA would understand that Go teaches the Preamble, to the extent that it is a limitation. For example, Figure 7 (annotated with the same color scheme identified above) depicts a “computer system [that] includes a computer body 30 having a video card 32 and a bus compressor 34, and an LCD 40 connected to the video card 32 and the bus compressor over an FPC cable 36”:
The above computer system is a “data transfer system” that converts “display data” from a video card into a multi-level signal using bus compressor 34 to ultimately provide display data for liquid crystal panel 42 (i.e. matrix display panel). (Ex. 1004 at Fig. 7, 3:32-35; see also Ex. 1009 at Claim 1[preamble]).

**[1a]** a multi-level timing controller for receiving a digital data input and converting it into a multi-level signal display data output;

65. It is my opinion that a POSITA would understand that Go teaches a multi-level encoder (i.e. bus compressor 34) which receives 18 bits of digital data input from video card 32 and converts it into 9 analog multi-level signals. (Ex.
1004 at 3:50-58 (“The bus compressor 34 compresses the 18-bit video data VD from the first data bus 31 to 9-analog signals. Specifically, the bus compressor 34 modulates 2 bit data from two bit lines of the first data bus 31 to a single analog signal having a different amplitude signal AMS in accordance with logical values of the 2 bit data.”), Fig. 7, 4:35-61, Fig. 8; Ex. 1009 at Claim [1a]).

66. It is my opinion that a POSITA would understand that Beers teaches a controller for converting digital data to a clocked multi-level signal for transferring over a bus (i.e. a “multi-level timing controller”). Specifically, as detailed above in VII(B), Beers teaches a “multi-level timing controller” that includes: (a) interface latches 6 and an I/O clock; and (b) a multi-level encoder (i.e. current source drivers 7). Beers teaches that the “multi-level timing controller” receives input at interface latches 6 based on the frequency set via PROC CLK or processor clock (Ex. 1005 [Beers] at Fig. 2, 5:57-66) and provides as an output digital bit pair A and B, which is clocked at the frequency set by the I/O clock. (Id. at Fig. 2, 5:57 – 6:7). Beers further teaches that the “multi-level timing controller’s” multi-level encoder (i.e. current source drivers 7) “uses the reference signal generated by reference generator 8 to perform the digital to analog conversion between digital bit pair A and B and analog output current iT.” (Ex. 1005 [Beers] at 4:51-54; see also Ex. 1005 [Beers] at 3:50-58, 4:31-58, Fig. 3, 6:29-30, 6:55-67, Fig. 11; Ex. 1009 at Claim [1a]). Accordingly, it is my opinion that Beers teaches a “multi-level timing
controller” for receiving a digital data input and converting it into a multi-level signal display data output (i.e. analog output current $i_T$).  *(See also Ex. 1009 at Claim [1a]).

67. It is my opinion that a POSITA would be motivated to substitute the multi-level encoder of Go with the multi-level timing controller of Beers for the reasons set forth in Section VIII(A)(2) of this Petition. Accordingly, it is my opinion that Go-Beers teaches the foregoing limitation.

*[1b] a multi-level signal bus having a plurality of data lines, connected to said multi-level timing controller, for transferring said multi-level signal display data from said multi-level timing controller; and*

68. It is my opinion that Go teaches a multi-level signal bus (i.e. FPC cable 36) having a plurality of data lines, connected to a multi-level encoder (i.e. bus compressor 34), for transferring said multi-level signal display data from said multi-level encoder. Specifically, Go teaches a bus compressor 34 which receives 18 bits of digital data input from video card 32 and converts it to nine analog signals that are transmitted over FPC cable 36. *(Ex. 1004 at 3:50-60 (“The bus compressor 34 compresses the 18-bit video data VD from the first data bus 31 to 9-analog signals. Specifically, the bus compressor 34 modulates 2 bit data from two bit lines of the first data bus 31 to a single analog signal having a different amplitude signal AMS in accordance with logical values of the 2 bit data. The 9-analog signals AMS generated by the bus compressor 34 in this manner are*
transferred to the LCD 40 over the FPC cable 36”), Fig. 7, 4:35-61, Fig. 8; Ex. 1009 at Claim [1b]).

69. It is my opinion that Beers teaches a multi-level signal bus (i.e. I/O bus 3) having a plurality of data lines, connected to said multi-level timing controller (§ VIII(A)(1)(1a)) for transferring said multi-level signal display data from said multi-level timing controller. Specifically, Beers teaches that current i_T (i.e. multi-level signal data from said multi-level timing controller) is transferred over a multi-level signal bus (i.e. I/O bus 3). (Ex. 1005 at Fig. 2, 3:50-58, 4:31-58, Fig. 3, 6:29-30, 6:55-67, Fig. 11; Ex. 1009 at Claim [1b]).

70. It is my opinion that a POSITA would be motivated to substitute the multi-level input data driver of Go with the multi-level input data driver of Beers for the reasons set forth in Section VIII(A)(2) of this Declaration. Accordingly, it is my opinion that Go-Beers teaches the foregoing limitation.

[1c] **a multi-level input data driver connected to said multi-level signal bus, for receiving said multi-level signal display data input and converting it into a data driving signal to be outputted to said matrix display panel.**

71. It is my opinion that Go teaches a multi-level input data driver (i.e. bus decompressor 46) connected to said multi-level signal bus (i.e. FPC cable 36), for receiving said multi-level signal display data input and converting it into a data driving signal to be outputted to said matrix display panel (i.e. liquid crystal panel 42). Specifically, Go teaches a bus decompressor 46 which receives nine analog
signals from FPC cable 36 and converts the nine analog signals to an 18 bit data
driving signal outputted to liquid crystal panel 42. (Ex. 1004 at 4:1-4, Fig. 7, 4:16-
19, 5:10 – 5:52, Fig. 10; Ex. 1009 at Claim [1c]).

72. It is my opinion that Beers teaches that the multi-level input signal
transferred over I/O bus 3 is received by multi-level converter 12, which is a multi-
level decoder. (See § Section VII(B)). Multi-level converter 12 converts the
multi-level signal, current $i_T$, into bits A and B (i.e. digital data). (Ex. 1005 [Beers]
at Fig. 2, 4:59 – 5:11, Fig. 4; 6:18-53, Fig. 10). Ultimately, bits A and B are
transferred to peripheral 2 through peripheral mux 11. (Ex. 1005 [Beers] at Fig. 2,
6:6-17, Fig. 9). Accordingly, it is my opinion that Beers teaches a “multi-level
input data driver” for receiving said multi-level signal display data input and
converting it into a data driving signal. (Ex. 1009 at Claim [1a]).

73. It is my opinion that Beers teaches a multi-level input data driver (i.e.
multilevel converter 12) connected to said multi-level signal bus (i.e I/O bus 3), for
receiving multi-level signal data input and converting it into a data driving signal
to be outputted to peripheral device 2. Specifically, Beers teaches that current $i_T$
(i.e. multi-level signal data from said multi-level timing controller) is transferred
over a multi-level signal bus (i.e. I/O bus 3) to a multi-level input data driver (i.e.
multilevel converter), which decodes $i_T$ into bits A and B. (Ex. 1005 [Beers] Fig.
2, 4:59 – 5:11, Fig. 4; 6:18-53, Fig. 10; Ex. 1009 at Claim [1c]). Beers further
teaches that Bits A and B are ultimately transferred to peripheral 2 through peripheral mux 11. (Ex. 1005 [Beers] at Fig. 2, 6:6-17, Fig. 9; Ex. 1009 at Claim [1c]).

74. It is my opinion that a POSITA would be motivated to substitute the multi-level input data driver of Go with the multi-level input data driver of Beers for the reasons set forth in Section VIII(A)(2) of this Petition. Accordingly, it is my opinion that Go-Beers teaches the foregoing limitation.

[CLAIM 2] The system according to claim 1, wherein said multi-level timing controller comprises a multi-level encoder for encoding said digital data input and said multi-level input data driver comprises a multi-level decoder for decoding said multi-level signal display data.

75. As discussed above, it is my opinion that Beers teaches “said multi-level timing controller comprises a multi-level encoder for encoding said digital data input.” (See § VIII(A)(1)(1a)). Further, it is my opinion that Go teaches “a multi-level encoder for encoding said digital data input.” (See § VIII(A)(1)(1a)). Go and Beers each teach “said multi-level input data driver comprises a multi-level decoder for decoding said multi-level signal display data.” (See § VIII(A)(1)(1c)). Accordingly, for the reasons discussed above in Sections VIII(A)(1)(1a & 1c), it is my opinion that Go-Beers teaches the foregoing limitation.

[CLAIM 3-PREAMBLE] A data transfer method for a multi-level signal for providing a display data to a matrix display panel, said method comprising the steps of:

76. Claim 3 is a method claim that requires the use of the same structural
components as system Claim 1 and is materially the same as merely using the
system of Claim 1. For example, the Preambles of Claims 1 and 3 are identical
except that the Preamble of Claim 3 replaces “system” with “method” and recites
“method comprising the steps of” with “comprising.” Accordingly, for the reasons
discussed above in Section VIII(A)(1)[CLAIM 1-PREAMBLE], it is my opinion
that Go-Beers teaches this limitation. (See also Ex. 1009 at Claim 1[preamble]).

[3a] converting a first digital data signal into a multi-level signal display data
output by a multi-level timing controller;

77. Claim 3 is a method claim that requires the use of the same structural
components as system Claim 1 and is materially the same as merely using the
system of Claim 1. For example, both claim limitation 1a and 3a require a multi-
level timing controller that converts a digital data input into a multi-level signal
display data output, but claim limitation 1a additionally requires that the multi-
level timing controller receive the digital data input. Accordingly, for the reasons
discussed above in Section VIII(A)(1)[1a], it is my opinion that Go-Beers teaches
this limitation. (See also Ex. 1009 at Claim [1a]).

[3b] transferring said multi-level signal display data by a multi-level signal
bus comprising a plurality of data lines; and

78. Claim 3 is a method claim that requires the use of the same structural
components as system Claim 1 and is materially the same as merely using the
system of Claim 1. For example, both claim limitation 1b and 3b require a “multi-
level signal bus” that has “a plurality of data lines” for “transferring said multi-level signal display data,” but claim limitation 1b additionally requires that the multi-level signal bus be connected to the multi-level timing controller and “transferring said multi-level signal display data from said multi-level timing controller.” Accordingly, for the reasons discussed above in Section VIII(A)(1)[1b], it is my opinion that Go-Beers teaches this limitation. (See also Ex. 1009 at Claim [1b]).

[3c] converting said multi-level signal display data input into a second digital data signal by a multi-level input data driver.

79. Claim 3 is a method claim that requires the use of the same structural components as system Claim 1 and is materially the same as merely using the system of Claim 1. For example, both claim limitation 1c and 3c require a “multi-level input data” for “converting said multi-level signal display data input into a … digital data signal,” but claim limitation 1c additionally requires that the multi-level input data driver be connected to the multi-level signal bus and further requires that the “digital driving signal … be outputted to said matrix display panel.” Also, claim limitation 3c identifies the “digital data signal” as a “second digital data signal.” Accordingly, for the reasons discussed above in Section VIII(A)(1)[1c], it is my opinion that Go-Beers teaches this limitation. (See also Ex. 1009 at Claim [1c]).
[CLAIM 4] The method according to claim 3, further comprising converting said second digital data signal into an analog signal.

80. It is my opinion that a POSITA would understand that a digital-to-analog converter ("DAC") is present in a conventional digital input data driver for an LCD display, and thus, would understand that Go teaches converting. To the extent it is alleged that it is not known to a POSITA, the ’247 APA shows that it was known in the prior art. Specifically, the ’247 Patent teaches that Figure 4 is “a schematic view of a conventional digital input driver on an LCD” and that “in a prior art digital input data driver 20 shown in FIG. 4, data from FIG. 3 passes through an input data register 22, an internal processing logic 24 and a digital-to-analog converter (DAC) to become an analog signal output, which is a data driving signal.” Thus, it is my opinion that a POSITA would understand that the input data driver in Go would include a DAC for converting said digital data signal into an analog signal. Accordingly, it is my opinion that Go teaches this limitation. (See also Ex. 1009 at Claim 4).

[CLAIM 5] The method according to claim 3, wherein step (a) comprises encoding said first digital data signal by a multi-level encoder, and step (c) comprises decoding said multi-level signal display data by a multi-level decoder.

81. Claim 3 is a method claim that requires the use of the same structural components as system Claim 1 and is materially the same as merely using the system of Claim 1. (See §§ VIII(A)(1)[Claim-PREAMBLE – 3c]). Claim 5
depends from Claim 3. Accordingly, for the reasons discussed above in Claim [1a] with respect to encoding a first digital data signal with a multi-level encoder (See § VIII(A)(1)[1a] ; see also Ex. 1009 at Claim [1a]) and for the reasons discussed above with respect to decoding multi-level signal display data with a multi-level decoder (See §VII(A)(1)[1c]; see also Ex. 1009 at Claim [1c]), it is my opinion that Go-Beers teaches this limitation.

[CLAIM 6-PREAMBLE] A liquid crystal display device, comprising:

82. Go teaches an LCD computer system comprising an LCD 40 connected to a computer body 30. (Ex. 1004 [Go] at Fig. 7, 3:12-14, 3:29-43; see also Ex. 1009 at Claim 6[preamble]). Accordingly, it is my opinion that Go teaches this limitation.

[6a] a matrix liquid crystal display panel:

83. Go teaches an LCD computer system comprising LCD 40 which itself comprises liquid crystal panel 42. (Ex. 1004 [Go] at Fig. 7, 3:12-14, 3:29-43; see also Ex. 1009 at Claim [6a]). Accordingly, it is my opinion that Go teaches this limitation.

[6b] a scan driver for providing a scan voltage signal to said liquid crystal display panel by a plurality of scan bus lines; and

84. It is my opinion that a POSITA would understand that scan drivers are present in every LCD display, and thus, would understand that Go teaches a scan driver for providing a scan voltage signal to said liquid crystal display panel by a
plurality of scan bus lines. To the extent it is alleged that it is not known to a POSITA, the ’247 APA shows that it was known in the prior art. Specifically, in the “Background of the Invention” section, the ’247 Patent states that a “conventional active matrix LCD” would include “a plurality of scan bus lines Y1, Y2, …, Yn” and a scan driver 10 for driving said scan bus lines. (Ex. 1001 [’247 APA] at 1:27-40, Fig. 1; see also Ex. 1009 at Claim [6b]). Accordingly, it is my opinion that Go teaches this limitation.

[6c] a display data transfer system for providing a data driving signal to said liquid crystal display panel by a plurality of data bus lines, said display data transfer system comprising:

85. It is my opinion that Go teaches a display data transfer system for providing a data driving signal to said liquid crystal display panel by a plurality of data bus lines. Specifically, Figure 7 of Go teaches “an LCD computer system” which “includes a number of D-ICs 44 for divisionally and selectively driving the pixels in the liquid crystal panel 42.” (Ex. 1004 [Go] at 3:12-13, 3:63-65, Fig. 7; see also 4:16-21; Ex. 1009 at Claim [6c]). Accordingly, it is my opinion that Go teaches this limitation.

[6d] a multi-level timing controller for receiving a digital data input and converting it into a multi-level signal display data output;

86. Claim limitation 6d is identical to Claim limitation 1a. Accordingly, for the reasons discussed above in Section VIII(A)(1)[1a], it is my opinion that Go-Beers teaches this limitation. (See also Ex. 1009 at Claim [1a]).
[6e] a multi-level signal bus having a plurality of data lines, connected to said multi-level timing controller, for transferring said multi-level signal display data from said multi-level timing controller; and

87. Claim limitation 6e is identical to Claim limitation 1b. Accordingly, for the reasons discussed above in Section VIII(A)(1)[1b], it is my opinion that Go-Beers teaches this limitation. (See also Ex. 1009 at Claim [1b]).

[6f] a multi-level input data driver connected to said multi-level signal bus, for receiving said multi-level signal display data input and converting it into said data driving signal.

88. Claim limitation 6f is identical to Claim limitation 1c. Accordingly, for the reasons discussed above in Section VIII(A)(1)[1c], it is my opinion that Go-Beers teaches this limitation. (See also Ex. 1009 at Claim [1c]).

[CLAIM 7] The device according to claim 6, wherein said multi-level timing controller comprises a multi-level encoder for encoding said digital data input and said multi-level input data driver comprises a multi-level decoder for decoding said multi-level signal display data.

89. As discussed above, it is my opinion that Beers teaches “said multi-level timing controller comprises a multi-level encoder for encoding said digital data input.” (See § VIII(A)(1)(1a)). Further, it is my opinion that Go teaches “a multi-level encoder for encoding said digital data input.” See § VIII(A)(1)(1a). It is my opinion that Go and Beers each teach “said multi-level input data driver comprises a multi-level decoder for decoding said multi-level signal display data.” See § VIII(A)(1)(1c). Accordingly, for the reasons discussed above in Sections VIII(A)(1)(1a & 1c) and Section VIII(A)(1)(6), it is my opinion that Go-Beers
teaches the foregoing limitation.

[CLAIM 8] The system according to claim 1, wherein said multi-level signal display data is in the form of digital signals with amplitudes equal to one of eight values.

  90. Go teaches the use of a “bus compressor 34 [that may be] used for compressing 3-bits of data.” (Ex. 1004 [Go] at 5:6-10; see also id. at 5:10 – 5:52, Fig. 10). A bus compressor that compresses 3-bits would create a multi-level signal with an amplitude equal to one of eight values. Accordingly, it is my opinion that Go teaches the foregoing limitation.

  91. Beers teaches the use “a 3-bit multilevel converter” whose input, “current i_T is a multilevel analog signal now coded to represent three binary bits, characterized in one of eight discrete levels.” (Ex. 1005 [Beers] at 6:18-42). Accordingly, it is my opinion that Beers teaches the foregoing limitation.

[CLAIM 9] The method according to claim 3, wherein said multi-level signal display data is in the form of digital signals with amplitudes equal to one of eight values.

  92. Claim 8 requires the same limitation as claim 9 but rather than depend from claim 3, claim 8 depends from claim 1. Accordingly, for the reasons set forth in Section VIII(A)(1)[CLAIM 8], it is my opinion that Go and Beers each disclose this limitation.

[CLAIM 10] The device according to claim 6, wherein said multi-level signal display data is in the form of digital signals with amplitudes equal to one of eight values.

  93. Claim 8 requires the same limitation as claim 10 but rather than
depend from claim 3, claim 8 depends from claim 1. Accordingly, for the reasons set forth in Section VIII(A)(1)[CLAIM 8], it is my opinion that Go and Beers each disclose this limitation.

2. Motivation to Combine

94. It is my opinion that a POSITA would have been motivated to combine Go and Beers (collectively, “Go-Beers”). Both references are directed to the transmission of data to peripheral devices, such as an LCD. Both references are directed to the design of multi-level interfaces for a peripheral device. Go describes the use of multi-level signals to transmit display data to a peripheral, i.e. an LCD. (Ex. 1004 [Go] at 3:32-35, 3:50-60). Beers similarly describes the use of multi-level signals to transmit data to peripheral devices generally. (Ex. 1005 [Beers] at 3:8-24).

95. In addition, both references teach that that EMI is a problem when transferring data on a bus at a high frequency. Go teaches that there are two factors that affect EMI: the number of wires or transmission lines on a bus and the transfer frequency. For example, Go teaches that, “[a]s the frequency band for the information and the number of transmission lines increases, an electromagnetic interference (EMI) increases between the transmission lines.” (Ex. 1004 [Go] at 1:22-25). Go teaches that this EMI stems from impedance mismatches related to the frequency and number of wires on the bus and also teaches that matching
impedances is one technique for reducing EMI. (Ex. 1004 [Go] at 1:22-34; 1:56-57, 6:17-46, 1:34-55). Similarly, Beers teaches, through its incorporated reference (Frankeny) (Ex. 1005 [Beers] at 1:7-14), that “[c]omputer system clock speeds continue to increase [and t]he measurement of data signals subject to change at such high frequencies is becoming more difficult because of impedance mismatch induced reflections on the connecting lines.” (Ex. 1008 [Frankeny] at 1:26-31; see also id. at 1:31-45; Ex. 1005 [Beers] at 1:7-14). It is my opinion that a POSITA would understand that these “impedance mismatch induced reflections” are a form of EMI. Thus, it is my opinion that Beers also teaches that it is desirable to solve the same EMI problem stemming from reflections and mismatching impedances. (Ex. 1008 [Frankeny] at 1:20-22, 1:25-60; Ex. 1005 [Beers] at 1:7-14).

96. To address the EMI problem, Go addresses one factor of EMI (i.e. number of wires) and teaches using multi-level signals to reduce the number of wires needed to transfer data over a bus. (1004 [Go] at 4:22-27, 6:25-32, 6:36-43). Beers addresses the other factor of EMI identified by Go (i.e. frequency (Ex. 1004 [Go] at 1:22-25)) and teaches that multi-level signals can be used to also reduce the transfer frequency to reduce EMI. (Ex. 1005 [Beers] at 3:8-24).

97. As explained in Section VI(C), it is my opinion that a “multi-level timing controller” is “a controller for converting digital data to a clocked multi-level signal for transferring over a bus.” As discussed in Section VIII(A)(1)[1a], it
is my opinion that Beers teaches a “multi-level timing controller” that includes an I/O clock, interface latches and a multi-level encoder (i.e. current source drivers) to transmit data on a multi-level bus that is clocked at a reduced frequency as compared to the frequency of the input data. (Ex. 1005 [Beers] at Fig. 2, 3:8-24). Accordingly, it is my opinion that a POSITA would understand that replacing the multi-level encoder of Go with the multi-level timing controller of Beers (which includes an I/O clock and interface latches in addition to a multi-level encoder) to reduce the transfer frequency (i.e. the EMI factor identified but not addressed in Go) would further reduce EMI. Thus, it is my opinion that a POSITA would understand that the combined Go-Beers device would address both factors of EMI to obtain the following benefits: (a) the ability to reduce both the numbers of wires needed to transfer data over a bus to reduce EMI; and (b) the ability to reduce the transfer frequency to additionally reduce EMI. Therefore, it is my opinion that a POSITA would understand this combination would be nothing more than a simple substitution of one known element for another known element to obtain predictable results (further reduce EMI).

Further, it is my opinion that a POSITA would have been motivated to combine both references because both references use known techniques (i.e. using multi-level signals to transmit data) to improve similar devices (i.e. peripherals in Beers and one type of peripheral—an LCD—in Go) in the same way (i.e. for the
same benefit: to reduce EMI).

99. Accordingly, it is my opinion that a POSITA would be motivated to combine both references as illustrated below, the material components of which are highlighted as follows:

- multi-level encoder of Go (i.e. bus compressor 34) (blue) is replaced by the multi-level timing controller of Beers (i.e. PROC CLK, Peripheral (I/O) CLK, interface latches 6, current source drivers 7 and reference generator 8, collectively) (blue)

- multi-level signal bus of Go (i.e. FPC cable 36) (yellow)

- multi-level input data driver of Go (i.e. bus decompressor 46) (pink) is replaced by the multi-level input data driver of Beers (i.e. peripheral mux 11, multilevel converter 12, reference replicator 13, collectively) (pink)

- Liquid crystal panel 42 of Go (green)
B. GROUND 2: Claims 1-10 are Obvious under 35 U.S.C. § 103(a) over Kuwata in view of Chen (collectively, “Kuwata-Chen”)

3. Challenged Claims

[CLAIM 1-PREAMBLE] A data transfer system for a multi-level signal for providing a display data to a matrix display panel, comprising:

100. It is my opinion that Kuwata teaches a data transfer system for providing a display data to a matrix display panel. Specifically, Kuwata teaches a “driving circuit 200 for a liquid crystal display device” (i.e. matrix display panel) (Ex. 1006 [Kuwata] at 4:39-47) that includes “[a] memory 130 consisting of VRAM [that] stores picture image data corresponding to one frame” (i.e. display data) that is provided for the liquid crystal display device (Id. at 4:5-67). It is my opinion that Chen teaches a data transfer system that includes an “advanced input/output interface allows for high speed/bandwidth memory accesses while reducing the pin count and operating frequency required for operation.” (Ex. 1007 [Chen] at Abstract).

101. It is my opinion that a POSITA would be motivated to combine the advanced input/output interface of Chen with the memory of Kuwata for the reasons set forth in Section VIII(B)(2) of this Petition. Accordingly, it is my opinion that Kuwata-Chen teaches the foregoing limitation.

1a. a multi-level timing controller for receiving a digital data input and converting it into a multi-level signal display data output;

102. It is my opinion that Chen teaches a multi-level timing controller (i.e.
BCC 24 and PLL Clock Generator, collectively) for receiving a digital data input and converting it into a multi-level signal display data output. (Ex. 1007 [Chen] at 8:19-23 (“BCC 24 generally functions to convert a plurality (i.e., n) of two-level protocol signals received over a respective bus 30 into a single, multi-level protocol signal which is output on a respective line 32.”).

[1b] a multi-level signal bus having a plurality of data lines, connected to said multi-level timing controller, for transferring said multi-level signal display data from said multi-level timing controller; and

103. It is my opinion that Chen teaches a multi-level signal bus (i.e. bus 22) having a plurality of data lines, connected to said multi-level timing controller (i.e. BCC 24 and PLL Clock Generator, collectively), for transferring said multi-level signal display data from said multi-level timing controller. (Ex. 1007 [Chen] at 7:12-17 (“For a multi-level protocol signal output by the respective BCC 24, each VGC circuit 28 outputs a controlled signal which is placed on bus 22 connecting to control device 14.”), Fig. 1; see also id. at Ex. 1010 at Claim [1b]).

As shown below, the multi-level signal bus (i.e. bus 22) of Chen is connected to the multi-level timing controller (i.e. BCC 24 and PLL Clock Generator, collectively) through bus 32 and VGC 28 (annotated in red):
a multi-level input data driver connected to said multi-level signal bus, for receiving said multi-level signal display data input and converting it into a data driving signal to be outputted to said matrix display panel.

It is my opinion that Chen teaches a multi-level decoder (i.e. BDC 38) connected to said multi-level signal bus (i.e. bus 22), for receiving said multi-level signal display data input and converting it into a digital signal. (Ex. 1007 [Chen] at Fig. 1, 7:6-17 (explaining that BDC 38, VGC 28 and line 32 are “substantially similar” to BDC 26, VGC 40 and line 32, respectively), 7:15-17 (“Each multi-level protocol signal input into a BDC 26 is generated by a respective VGC circuit 28 in response to a signal received over bus 22.”), 9:26-30 (“BDC 26 functions to
convert a single multiplexed signal (D'k) formatted in a multi-level protocol and received over line 32 into a plurality of respective two-level protocol signals (D'k(0)-D'k(n−1)).”); *see also id. at Ex. 1010 at Claim [1c]). As shown below, the multi-level signal bus (i.e. bus 22) of Chen is connected to the multi-level input data driver (i.e. BDC 36) through bus 44 and VGC 40 (annotated in red):

105. It is my opinion that Kuwata teaches an input data driver (i.e. format converter 190, column voltage signal generator 180, row voltage signal generator 7 and driver control circuit 60, collectively) which receives digital data and converts it into a data driving signal to be outputted to a matrix display panel (i.e. liquid
crystal display panel). (Ex. 1006 [Kuwata] at Fig. 15, 11:4-5, 4:65-5:16).

106. The combination of multi-level decoder of Chen and the input data driver of Kuwata would create a multi-level input data driver that is connected to said multi-level signal bus (bus 22) and converts multi-level signal display data input received from the multi-level signal bus into a data driving signal that is outputted to the matrix display panel. It is my opinion that a POSITA would be motivated to combine Chen’s advanced input/output interface for memory with the memory of Kuwata for the reasons set forth in Section VIII(B)(2) of this Petition. Accordingly, it is my opinion that Kuwata-Chen teaches the foregoing limitation.

[CLAIM 2] The system according to claim 1, wherein said multi-level timing controller comprises a multi-level encoder for encoding said digital data input and said multi-level input data driver comprises a multi-level decoder for decoding said multi-level signal display data.

107. As discussed above, it is my opinion that Chen teaches “said multi-level timing controller comprises a multi-level encoder for encoding said digital data input.” (See § VIII(B)(1)(1a)). Further, it is my opinion that the combination of Chen and Kuwata teaches a multi-level input data driver that comprises a multi-level decoder for decoding said multi-level signal display data. See § VIII(B)(1)(1c). Accordingly, for the reasons discussed above in Sections VIII(B)(1)(1a & 1c), it is my opinion that Kuwata-Chen teaches the foregoing limitation.
[CLAIM 3-PREAMBLE] A data transfer method for a multi-level signal for providing a display data to a matrix display panel, said method comprising the steps of:

108. Claim 3 is a method claim that requires the use of the same structural components as system Claim 1 and is materially the same as merely using the system of Claim 1. Accordingly, for the reasons discussed above in Section VIII(B)(1)[CLAIM 1-PREAMBLE], it is my opinion that Kuwata-Chen teaches this limitation. (See also Ex. 1010 at Claim [1a]).

[3a] converting a first digital data signal into a multi-level signal display data output by a multi-level timing controller;

109. Claim 3 is a method claim that requires the use of the same structural components as system Claim 1 and is materially the same as merely using the system of Claim 1. Accordingly, for the reasons discussed above in Section VIII(B)(1)[1a], it is my opinion that Kuwata-Chen teaches this limitation. (See also Ex. 1010 at Claim [1a]).

[3b] transferring said multi-level signal display data by a multi-level signal bus comprising a plurality of data lines; and

110. Claim 3 is a method claim that requires the use of the same structural components as system Claim 1 and is materially the same as merely using the system of Claim 1. Accordingly, for the reasons discussed above in Section VIII(B)(1)[1b], it is my opinion that Kuwata-Chen teaches this limitation. (See also Ex. 1010 at Claim [1b]).
[3c] converting said multi-level signal display data input into a second digital data signal by a multi-level input data driver.

111. Claim 3 is a method claim that requires the use of the same structural components as system Claim 1 and is materially the same as merely using the system of Claim 1. Accordingly, for the reasons discussed above in Section VIII(B)(1)[1c], it is my opinion that Kuwata-Chen teaches this limitation. (See also Ex. 1010 at Claim [1c]).

[CLAIM 4] The method according to claim 3, further comprising converting said second digital data signal into an analog signal.

112. It is my opinion that Kuwata teaches that the second digital data signal (i.e. the output of the multi-level input data driver) is converted into an analog signal. As discussed above in Sections VIII(B)(1)(1c & 3c), the combination of Kuwata-Chen includes the input data driver of Kuwata that further includes format converter 190. Kuwata teaches that “[t]he column voltage signal generator 180 produces voltage values to be applied to column electrodes based on a row selection pattern from a row selection pattern generator 7 and the output of the format convertor 190.” (Ex. 1006 [Kuwata] at 5:4-8). In the Background of the Invention section, Kuwata further teaches two examples of voltage patterns applied to a column electrode showing column electrode voltages, and these voltages included -4, -2, 2 and 0. (Ex. 1006 [Kuwata] at Fig. 14, 1:48-65, 1:33-47). It is my opinion that a POSITA would understand that these voltages (i.e. -4, -2, 2 and
0) represent an analog signal applied to a column electrode because there are more than two values of voltages applied and a digital signal would be limited to a binary signal (i.e. two voltage values). Since Kuwata-Chen teaches converting the digital signal from format converter 190 into an analog signal that is applied to a column electrode, it is my opinion that Kuwata-Chen teaches this limitation.

[CLAIM 5] The method according to claim 3, wherein step (a) comprises encoding said first digital data signal by a multi-level encoder, and step (c) comprises decoding said multi-level signal display data by a multi-level decoder.

113. As discussed above, it is my opinion that Chen teaches a multi-level timing controller that comprises a multi-level encoder for encoding said digital data input.” (See § VIII(B)(1)(1a)). Further, it is my opinion that the combination of Chen and Kuwata teaches a multi-level input data driver that comprises a multi-level decoder for decoding said multi-level signal display data. See § VIII(B)(1)(1c). Accordingly, for the reasons discussed above in Sections VIII(B)(1)(1a & 1c), it is my opinion that Kuwata-Chen teaches the foregoing limitation, which requires encoding said first digital data signal by a multi-level encoder in step (a) and decoding said multi-level signal display data by a multi-level decoder in step (c).

[CLAIM 6-PREAMBLE] A liquid crystal display device, comprising:

114. It is my opinion that Kuwata teaches a liquid crystal display device, namely a personal computer with an LCD. (Ex. 1006 [Kuwata] at Fig. 15, 4:39-47,
Accordingly, it is my opinion that Kuwata teaches this limitation.

[6a] **a matrix liquid crystal display panel:**

115. It is my opinion that Kuwata teaches a matrix liquid crystal display panel (i.e. liquid crystal display panel 40). (Ex. 1006 [Kuwata] at Fig. 15, 4:39-47, 11:4-5). Accordingly, it is my opinion that Kuwata teaches this limitation.

[6b] **a scan driver for providing a scan voltage signal to said liquid crystal display panel by a plurality of scan bus lines; and**

116. It is my opinion that Kuwata teaches a scan driver (i.e. row drivers 90) for providing a scan voltage signal to said liquid crystal display panel (i.e. liquid crystal display panel 40) by a plurality of scan bus lines (bus between row drivers 90 and liquid crystal display panel 40). (Ex. 1006 [Kuwata] at Fig. 15, 4:39-47, 11:4-5, 5:9-11 (“The row selection pattern from the row selection pattern generator 7 is supplied also to row drivers 90.”), 5:11-14 (The column drivers 80 and the row drivers 90 drive column electrodes and row electrodes of a liquid crystal display pattern 40 based on the inputted signals.”), 5:14-16 (“A driver control circuit 60 controls a driving timing to the column drivers 80 and the row drivers 90.”). Accordingly, it is my opinion that Kuwata teaches this limitation.
[6c] a display data transfer system for providing a data driving signal to said liquid crystal display panel by a plurality of data bus lines, said display data transfer system comprising:

117. Kuwata teaches a display data transfer system for providing a data driving signal to said liquid crystal display panel by a plurality of data bus lines. Specifically, Kuwata teaches an LCD driver circuit 200 that “produces voltage values [that are] supplied to the column drivers 80” and further teaches that “column drivers 80 … drive column electrodes … of a liquid crystal display pattern 40 based on the inputted signals.” (Ex. 1006 [Kuwata] at 5:1-16, Fig. 15; see also Ex. 1010 at Claim [6c]). Accordingly, Kuwata teaches this limitation.

[6d] a multi-level timing controller for receiving a digital data input and converting it into a multi-level signal display data output;

118. Claim limitation 6d is identical to Claim limitation 1a. Accordingly, for the reasons discussed above in Section VIII(B)(1)[1a], it is my opinion that Kuwata-Chen teaches this limitation. (See also Ex. 1010 at Claim [1a]).

[6e] a multi-level signal bus having a plurality of data lines, connected to said multi-level timing controller, for transferring said multi-level signal display data from said multi-level timing controller; and

119. Claim limitation 6e is identical to Claim limitation 1b. Accordingly, for the reasons discussed above in Section VIII(B)(1)[1b], it is my opinion that Kuwata-Chen teaches this limitation. (See also Ex. 1010 at Claim [1b]).
[6f] a multi-level input data driver connected to said multi-level signal bus, for receiving said multi-level signal display data input and converting it into said data driving signal.

120. Claim limitation 6f is identical to Claim limitation 1c. Accordingly, for the reasons discussed above in Section VIII(B)(1)[1c], it is my opinion that Kuwata-Chen teaches this limitation. (See also Ex. 1010 at Claim [1c]).

CLAIM 7] The device according to claim 6, wherein said multi-level timing controller comprises a multi-level encoder for encoding said digital data input and said multi-level input data driver comprises a multi-level decoder for decoding said multi-level signal display data.

121. As discussed above, it is my opinion that Chen teaches a multi-level timing controller that comprises a multi-level encoder for encoding said digital data input.” (See § VIII(B)(1)(1a)). Further, it is my opinion that the combination of Chen and Kuwata teaches a multi-level input data driver that comprises a multi-level decoder for decoding said multi-level signal display data. See § VIII(B)(1)(1c). Accordingly, for the reasons discussed above in Sections VIII(B)(1)(1a & 1c) and Section VIII(B)(1)(6), it is my opinion that Kuwata-Chen teaches the foregoing limitation.

[CLAIM 8] The system according to claim 1, wherein said multi-level signal display data is in the form of digital signals with amplitudes equal to one of eight values.

122. Chen teaches that each BCC 24 (i.e. multi-level encoder) “has a compression rate of n-to-1--i.e., compressing n two-level protocol signals from timing generator and data path circuitry 18 into a single, multi-level protocol
signal.” (Ex. 1007 [Chen] at 6:22-25). Chen further teaches that, “[f]or this compression, the number of distinct signal levels needed in the multi-level protocol signal is $2^n$.” Chen also teaches that this compression protocol may be used compress “at least two bits of information” into a single multi-level signal. (Ex. 1007 [Chen] at 3:6-9 (“Such protocol is a multi-level protocol which uses more than two voltage levels for signaling, wherein each voltage level represents a predetermined set of values for at least two bits of information.”), 6:18-21, 6:22-25). Thus, it is my opinion that a POSITA would understand that Chen teaches a BCC 24 may be used to compress more than two bits, such as three bits, into a single multi-level signal and would require $2^3$ or 8 distinct signal values. Accordingly, it is my opinion that Chen teaches this limitation.

[CLAIM 9] The method according to claim 3, wherein said multi-level signal display data is in the form of digital signals with amplitudes equal to one of eight values.

123. Claim 8 requires the same limitation as claim 9 but rather than depend from claim 3, claim 8 depends from claim 1. Accordingly, for the reasons set forth in Section VIII(B)(1)[CLAIM 8], it is my opinion that Chen teaches this limitation.

[CLAIM 10] The device according to claim 6, wherein said multi-level signal display data is in the form of digital signals with amplitudes equal to one of eight values.

124. Claim 8 requires the same limitation as claim 10 but rather than depend from claim 3, claim 8 depends from claim 1. Accordingly, for the reasons
set forth in Section VIII(B)(1)[CLAIM 8], it is my opinion that Chen teaches this limitation.

4. **Motivation to Combine**

125. It is my opinion that a POSITA would have been motivated to combine Kuwata and Chen (collectively, “Kuwata-Chen”). Both references relate to the transfer of data to and from memory. For example, Kuwata includes a “conventional driver circuit for a liquid crystal device” (Ex. 1006 [Kuwata] at 11:4-5) which includes a “memory 130 consisting of VRAM stores picture image data corresponding to one frame” (Ex. 1006 [Kuwata] at 4:55-57) and control logic that requests, receives and processes the data in memory 130 (Ex. 1006 [Kuwata] at 4:57-67). Chen teaches an “advanced input/output interface allows for high speed/bandwidth memory accesses” (Ex. 1007 [Chen] at Abstract) that is embodied in Figure 1 and includes a control device 14, which “transfers data and other information to and from memory device 12 for control, addressing, processing, and other operations” *(Id. at 7:37-40)*.

126. Kuwata teaches that the prior art driver circuit of Figure 15 had two problems: (1) “the VRAM used as the memory 130 is relatively expensive whereby the driving circuit can not be constituted economically”; and (2) “the driving circuit have a problem that power consumption rate and radiation noise are relatively large because memory access is necessary at a high speed.” *(Ex. 1006*
It is my opinion that a POSITA would understand that the radiation noise of Kuwata is EMI. Kuwata further teaches an invention that, in contrast to the prior art driver circuit of Figure 15 that uses relatively expensive VRAM, instead “provide[s] a driving circuit for a liquid crystal display device of low cost in which DRAMs are used.” (Ex. 1006 [Kuwata] at 5:22-33).

127. Chen teaches an advanced I/O interface with a memory device that addresses both problems of the Kuwata prior art while providing the “high speed” memory access that is necessary for a driving circuit. Specifically, Chen teaches an advanced I/O interface that “allows for high speed/bandwidth memory accesses while reducing the pin count and operating frequency required for operation.” (Ex. 1007 [Chen] at Abstract (emphasis added)). Chen further teaches that “reducing the number of pins and the clock frequency which would otherwise be required to transfer information to and from an IC memory device … minimizes the package pin-count, and hence, the EMI on a PC board, for high-bandwidth memory applications.” (Id. at 3:56-61 (emphasis added)). Chen additionally teaches that “[a] small pin count and low operating frequency are extremely desirable for system applications where portability and power-consumption are primary concerns.” (Id. at 3:61-64; see also 6:66 – 7:2). Thus, it is my opinion that a POSITA would understand that Chen teaches an advanced I/O interface that allows for high speed memory accesses while minimizing EMI and power consumption.
Accordingly, it is my opinion that a POSITA would be motivated to combine the prior art driver circuit disclosed in Figure 15 of Kuwata with the advanced I/O interface shown of Chen by replacing memory 130 of Kuwata with the advanced I/O interface containing memory device 12 shown in Figure 1 of Chen to provide high speed memory accesses while reducing the power consumption and EMI problem of Figure 15 of Kuwata.

128. In addition, Chen teaches an advanced I/O interface that includes memory device 12, which can be “any suitable integrated circuit (IC) memory device” and, like the low cost invention of Kuwata, this “includ[es] dynamic random access memory (DRAM).” (Ex. 1007 [Chen] at Fig. 1, 4:42-52; Ex. 1006 [Kuwata] at 5:30-33). Accordingly, it is my opinion that a POSITA would be motivated to combine Kuwata and Chen by replacing the VRAM of memory 130 with the advanced I/O interface shown in Figure 1 of Chen containing memory device 12, which includes DRAM, to provide a low cost driver circuit.

129. It is my opinion that a POSITA would be able to replace memory 130 of Kuwata with Figure 1 of Chen and configure memory device 12 in Figure 1 of Chen to perform the same functions as those of memory 130 without undue technological hurdles.

130. Further, it is my opinion that a POSITA would understand this combination would be nothing more than a simple substitution of one known
element (the VRAM of Kuwata, memory 130) for another known element (the advanced I/O interface of Chen, which can be used with DRAM) to obtain predictable results (reduce EMI and power consumption while maintaining high speed memory accesses).

131. Accordingly, it is my opinion that a POSITA would be motivated to combine both references as below, replacing memory 130 in Figure 15 of Kuwata with the integrated circuit memory device and control device of Chen:
132. All statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true. I further understand that willful false statements and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code. I
declare under penalty of perjury that the foregoing is true and correct.

Dated: February 9, 2017

Respectfully submitted,

[Vijay Madisetti, Ph.D.]

Vijay Madisetti, Ph.D.
Appendix A
Dr. Vijay K. Madisetti  
Fellow, IEEE  
vkm@madisetti.com  
Cell: 770-527-0177  
Address:  
56 Creekside Park Drive  
Johns Creek, GA 30022

Employment:

- 1984-1989: Post Graduate Researcher (UC Berkeley),  
- 1989-present: Full Professor of Electrical & Computer Engineering (Georgia Tech, Atlanta, GA 30332).


Startup Companies:

Director, VP Technologies, Inc. (1995- Present): A startup commercialized through Georgia Tech’s Advanced Technology Development Corporation (ATDC) focusing on digital software and hardware design services for military market. http://www.vptinc.com


Litigation Experience (2011-2016) With Testimony

**Case Name: HTC v. IPCOM**
Case No: 1:2008-cv-01897 (District of Columbia)
Expert for IPCOM.
(3G Standards: 2009 – 2012)
Testified by deposition

**Case Name: Apple v. Kodak**
Case No. ITC 337-TA-717 (ITC)
Expert for Kodak
(Digital Image Processing & UI: 2008-2011)
Testified at trial

**Case Name: Harkabi v. Sandisk,**
Case No: 1:08-cv-08203-WHP
Expert for Harkabi
(Digital Rights Management for Flash Devices: 2010-2012)
Testified at trial

**Case Name: Yangaroo Inc. v. Destiny Media Technologies, Inc.**
Case No: 09-C-0462
Expert for Yangaroo.
(Digital Rights Management Streaming: 2010-2011)
Testified by deposition

**Case Name: Motorola v. Microsoft,**
Case No: ITC 337-TA-752
Expert for Motorola
(Peer to Peer Gaming: 2011-2013)
Testified at trial

**Case Name: Motorola v. Apple,**
Case No: ITC 337-TA-745
Expert for Motorola
(Mobile Applications & UI: 2011-2012)
Testified at trial

**Case Name: Innovative Sonic Ltd. vs. RIM**
Case No: 3:11-cv-00706-K-BF
Expert for Innovative Sonic Ltd  
(3G Standards – Encryption, HSDPA: 2010-2013)  
Testified at trial

**Case Name: Interdigital v. ZTE, Huawei, Nokia (JDA)**  
Case No: ITC 337-TA-800  
Expert for JDA  
(3G Standards – HSDPA: 2012-2013)  
Testified at trial

**Case Name: Kodak v. Apple, HTC**  
Case No: ITC 337-TA-831  
Expert for Kodak  
(Digital Image Processing & UIs: 2011-2012)  
Submitted reports

**Case Name: Calypso v. T-Mobile**  
Case No: 2:08-CV-441-JRG-RSP  
Expert for T-Mobile  
(Unified Communications: 2012-2013)  
Testified by deposition

**Case Name: TracBeam v. AT&T**  
Case No: 6:11-cv-00096-LED  
Expert for AT&T  
(GPS Services: 2011-2012)  
Testified by deposition

**Case Name: BT v. Cox/Comcast**  
Case No: 10-658 (SLR) Delaware  
Expert for Cox and Comcast  
(VOIP, Network Management: 2012-2014)  
Testified by deposition

**Case Name: Ericsson v. Samsung**  
Case No: 337-TA-862 (ITC)  
Expert for Ericsson  
(RF Receivers, EDGE Standards: 2012-2013)  
Testified at trial

**Case Name: IPR – ContentGuard v. ZTE**  
Expert for ZTE  
(DRM for Digital Devices: 2012-2014)  
Testified by deposition

**Case Name: Emblaze v. Apple**
Case No: 5:11-cv-01079-PSG
Expert for Emblaze
(Digital Video/Audio Streaming: 2012-2014)
Testified at trial

**Case Name: Emblaze v. Microsoft**
Case No: 3:12-cv-05422-JST
Expert for Emblaze
(Digital Video/Audio Streaming: 2012 - Present)
Ongoing

**Case Name: MMI v. RIM**
Case No: 2:10-cv-00113-TJW-CE
Expert for MMI
(Area: Mobile Devices/User Interfaces: 2012-2013)
Testified by deposition

**Case Name: Wi-LAN v. Apple**
Case No: 13-cv-0790 DMS
Expert for Wi-LAN
Testified by Deposition

**Case Name: Sentius LLC v. Microsoft**
Case No: 5:13-cv-00825-PSG
Expert for Sentius
Testified by deposition

**Case Name: Medius Eagle Harbor v. Ford**
Case No: 3:1-cv-05503-BHS
Expert for Medius Tech
(Area: Automotive Multimedia Systems: 2014-)
Testified at Trial

**Genband US LLC v. Metaswitch Networks**
No 2:14-cv-33 (ED Texas Marshall)
Expert for Metaswitch Networks
Submitted declarations & deposition

**Enterprise - Systems Technologies S.a.r.l v. Samsung Electronics Co. Ltd**
Case No: 6:14-cv-555-MHS and ITC Inv. No. 337-TA-925
Expert for Samsung
Testified by deposition

**Ericsson Inc. v. Apple Inc.**
Case No: 2:15-cv-287 (ED Texas) and ITC-337-952/953
Expert for Ericsson
Testified by deposition & Trial

**Intellectual Ventures LLC v. Motorola Mobility LLC (Google)**
Case No: 13-cv-61358-RST (SD Florida)
Expert for Google
Testified by deposition (IPR)

**Intellectual Ventures LLC v. Nikon Corp**
C.A No. 11-1025-SLR (Delaware)
Expert for Nikon
Submitted declarations

**Masimo v. Mindray Biomedical Electronics Co.**
Case No: SACV-12-02206 CJC (JPRx) C. D. California
8:12-cv-02206-CJC-JPR
Expert for Masimo
Technology: Pulse Oximetry (2014 – present)
Submitted reports, testified by deposition

**Samsung v. Nvidia**
Case No: 3:14-cv-757-REP ED Virginia
Expert for Samsung
Technology: Microprocessors & Memories (2014 – present)
Submitted reports & Deposition & Trial

**Chrimar v. HP/Cisco/Alcatel**
Case No: 4:13-cv-1300-JSW
Expert for Chrimar
Technology: Power over Ethernet
Submitted reports & Deposition & Trial

Earned Degrees

1. **B. Tech (Hons), Electronics & Electrical Comm. Engineering**
   *Indian Institute of Technology (IIT), Kharagpur, India*
   1984.

2. **Ph.D., Electrical Engineering & Computer Sciences (EECS)**
   *University of California (UC), Berkeley, CA*
   1989.

Books

1. **VLSI Digital Signal Processors**
   *Madisetti, V.K.*

2. **Quick-Turnaround ASIC Design in VHDL**
   *Romdhane, M., Madisetti, V.K., Hines, J.*

   *Madisetti, V. K., Williams, D. (Editors)*

4. **VHDL: Electronics Systems Design Methodologies.**
   *Madisetti, V. K. (Editor)*

5. **Platform-Centric Approach to System-on-Chip (SoC) Design.**
   *Madisetti, V. K., Arpnikanondt, A.*
   Madisetti, V. K. (2009)
   CRC Press, Boca Raton, Fla.

   A Bahga, V. Madisetti (2013)

8. **Internet of Things: A Hands-On Approach**
   A Bahga, V. Madisetti (2014)
   *A. Bahga, V. Madisetti (2016)*  

**Edited Books & Collection of Papers**

1. **Advances in Parallel & Distributed Simulation**  
   *Madisetti, V.K.; Nicol, D., Fujimoto, R. (Editors)*  

2. **Modeling, Analysis, Simulation of Computer & Telecommunications Systems**
3. Modeling & Simulations on Microcomputers
   Madisetti, V.K. (Editor)

Editorship of Journals & Transactions

1. IEEE Design & Test of Computers
   Special Issue: Reengineering Digital Systems
   April – June 1999 (Vol 16, No 2)
   Madisetti, V.K. (Editor)

2. IEEE Design & Test of Computers
   Special Issue: Rapid Prototyping of Digital Systems
   Fall 1996 (Vol 13, No 3)
   Madisetti, V., Richards, M. (Editors)

3. IEEE Transactions on Circuits & Systems II
   Associate Editor: 1993-1995.

4. International Journal in Computer Simulation
   Associate Editor: 1990-1993

5. International Journal in VLSI Signal Processing
   Editorial Board: 1995 – Present

Refereed Journal Publications

1. Trends in the Electronic Control of Mine Hoists
   Madisetti, V. and Ramlu, M.,
   IEEE Transactions on Industry Applications, Vol IA-22, No. 6,
   November/December 1986. Pages 1105-1112
2. **Multilevel range/NEXT performance in digital subscriber loops**  
*Brand, G.; Madisetti, V.; Messerschmitt, D.G.*;  
Communications, Speech and Vision, IEE Proceedings I [see also IEE Proceedings-Communications] ,Volume: 136 , Issue: 2 , April 1989  
Pages:169 – 174

3. **Seismic migration algorithms on parallel computers**  
*Madisetti, V.K.; Messerschmitt, D.G.*;  
Pages:1642 – 1654

4. **Asynchronous algorithms for the parallel simulation of event-driven dynamical systems**  
*Madisetti, V.K.; Walrand, J.C.; Messerschmitt, D.G.*;  
ACM Transactions on Modeling and Computer Simulation, v 1, n 3, July 1991,  
Pages:  244-74

5. **Synchronization mechanisms for distributed event-driven computation**  
*Madisetti, V.K.; Hardaker, D.*;  
ACM Transactions on Modeling and Computer Simulation, v 2, n 1, Jan. 1992,  
Pages:  12-51

6. **Efficient VLSI Architectures for the Arithmetic Fourier Transform (AFT)**  
*Kelley, B.T.; Madisetti, V.K.*;  
Pages:365-378

7. **The fast discrete Radon transform. I. Theory**  
*Kelley, B.T.; Madisetti, V.K.*;  
Image Processing, IEEE Transactions on ,Volume: 2 , Issue: 3 , July 1993  
Pages:382 – 400

8. **The Georgia Tech digital signal multiprocessor**  
*Barnwell, T.P., III; Madisetti, V.K.; McGrath, S.J.A.*;  
Pages:2471 – 2487

9. **The MIMDIX Environment for Parallel Simulation**
10. **LMSGEN: a prototyping environment for programmable adaptive digital filters in VLSI**  
   Romdhane, M.S.B.; Madisetti, V.K.;  
   Chapter in VLSI Signal Processing, VII, 1994.,  
   Pages:33 – 42

11. **Fixed-point co-design in DSP**  
   Egolf, T.W.; Famorzadeh, S.; Madisetti, V.K.;  
   Chapter in VLSI Signal Processing, VII, 1994.,  
   Pages:113 - 126

12. **A fast spotlight-mode synthetic aperture radar imaging system**  
   Madisetti, V.K.;  
   Pages:873 – 876

13. **Rapid prototyping on the Georgia Tech digital signal multiprocessor**  
   Curtis, B.A.; Madisetti, V.K.;  
   Pages:649 – 662

14. **Low-power signaling in asymmetric noisy channels via spectral shaping**  
   Sipitca, M.; Madisetti, V.K.;  
   Pages:117 – 118

15. **A quantitative methodology for rapid prototyping and high-level synthesis of signal processing algorithms**  
   Madisetti, V.K.; Curtis, B.A.;  
   Pages:3188 – 3208

16. **Computer Simulation of Application-Specific Signal Processing Systems**  
   Casinovi, G.; Madisetti, V.K.;  
17. System partitioning of MCMs for low power
   *Khan, S.A.; Madisetti, V.K.*;
   Design & Test of Computers, IEEE ,Volume: 12 , Issue: 1 , Spring 1995
   Pages:41 – 52

18. Error correcting run-length limited codes for magnetic recording
   *Jaejin Lee; Madisetti, V.K.*;
   Pages:3084 – 3086

19. Virtual prototyping of embedded microcontroller-based DSP systems
   *Madisetti, V.K.; Egolf, T.W.*;
   Pages:9 – 21

20. Constrained multitrack RLL codes for the storage channel
   *Lee, J.; Madisetti, V.K.*;
   Pages:2355 – 2364

   *Madisetti, V.K.*;
   Design & Test of Computers, IEEE ,Volume: 13 , Issue: 3 , Fall 1996
   Pages:12 – 22

22. Conceptual prototyping of scalable embedded DSP systems
   *Dung, L.-R.; Madisetti, V.K.*;
   Design & Test of Computers, IEEE ,Volume: 13 , Issue: 3 , Fall 1996
   Pages:54 – 65

23. Advances in rapid prototyping of digital systems
   *Madisetti, V.K.; Richards, M.A.*;
   Design & Test of Computers, IEEE ,Volume: 13 , Issue: 3 , Fall 1996
   Pages:9

24. Combined modulation and error correction codes for storage channels
   *Jaejin Lee; Madisetti, V.K.*;
   Pages:509 – 514

25. Model-based architectural design and verification of scalable embedded DSP systems-a RASSP approach
   *Dung, L.-R.; Madisetti, V.K.; Hines, J.W.*;
Chapter in VLSI Signal Processing, IX, 1996. 
Pages:147 – 156

26. Low-power digital filter implementations using ternary coefficients  
Hezar, R.; Madisetti, V.K.; 
Chapter in VLSI Signal Processing, IX, 1996. 
Pages:179 – 188

27. All-digital oversampled front-end sensors  
Romdhane, M.S.B.; Madisetti, V.K.; 
Pages:38 – 39

28. Modeling COTS components in VHDL  
Calhoun, S., Reese, R; Egolf, T., Madisetti, V.K.; 
Pages: 24 – 31

29. VHDL-Based Rapid Systems Prototyping  
Egolf, T.; Madisetti, V.K.; 
Pages: 40-52

30. Interface design for core-based systems  
Madisetti, V.K.; Lan Shen; 
Pages:42 - 51

31. Incorporating cost modeling in embedded-system design  
Debardelaben, J.A.; Madisetti, V.K.; Gadient, A.J.; 
Pages:24 – 35

32. On homomorphic deconvolution of bandpass signals  
Marenco, A.L.; Madisetti, V.K.; 
Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and 
Pages:2499 – 2514

33. A case study in the development of multi-media educational material: the VHDL interactive tutorial  
Salinas, M.H.; Madisetti, V.K.; Egolf, T.; Famorzadeh, S.; Karns, L.N.; Carter, 
H.W.;
34. **Adaptive mobility management in wireless networks**  
*Jeongwook Kim; Madisetti, V.K.*;  
Pages: 1453 – 1455

35. **Efficient implementation of two-band PR-QMF filterbanks**  
*Hezar, R.; Madisetti, V.K.*;  
Pages: 92 – 94

36. **On fast algorithms for computing the inverse modified discrete cosine transform**  
*Yun-Hui Fan; Madisetti, V.K.; Mersereau, R.M.*;  
Pages: 61 – 64

37. **System on chip or system on package?**  
*Tummala, R.R.; Madisetti, V.K.*;  
Design & Test of Computers, IEEE , Volume: 16 , Issue: 2 , April-June 1999  
Pages: 48 – 56

38. **Reengineering legacy embedded systems**  
*Madisetti, V.K.; Jung, Y.-K.; Khan, M.H.; Kim, J.; Finnessy, T.*;  
Design & Test of Computers, IEEE , Volume: 16 , Issue: 2 , April-June 1999  
Pages: 38 – 47

39. **Reengineering digital systems**  
*Madisetti, V.K.*;  
Design & Test of Computers, IEEE , Volume: 16 , Issue: 2 , April-June 1999  
Pages: 15 – 16

40. **Parameter optimization of robust low-bit-rate video coders**  
*Sangyoun Lee; Madisetti, V.K.*;  
Circuits and Systems for Video Technology, IEEE Transactions on, Volume: 9  
Issue: 6 , Sept. 1999  
Pages: 849 – 855

41. **Closed-form for infinite sum in bandlimited CDMA**  
*Jatunov, L.A.; Madisetti, V.K.*;  
Communications Letters, IEEE , Volume: 8 , Issue: 3 , March 2004  
Pages: 138 – 140
42. A new protocol to enhance path reliability and load balancing in mobile ad hoc networks
   Argyriou, A.; Madisetti, V.K.;
   Journal of Ad Hoc Networks, Elsevier Press, 2004

43. Closed-form analysis of CDMA systems using Nyquist pulse
   Jatunov, L.A.; Madisetti, V. K.;

44. Systematic Design of End-to-End Wireless Mobility Management Protocols,
   Argyriou, A.; Madisetti, V. K.;
   ACM/Springer Wireless Networks (WINET), Accepted 2005.

45. A Novel End-to-End Approach for Video Streaming Over the Internet,
   Argyriou, A.; Madisetti, V. K.;

46. An Analytical Framework of RD Optimized Video Streaming with TCP,
   Argyriou, A.; Madisetti, V. K.;

47. Modeling the Effect of Handoffs on Transport Protocol Performance,
   Argyriou, A.; Madisetti, V. K.;
   IEEE Transactions on Mobile Computing, Submitted for review in March 2005

48. Throughput Models for Transport Protocols with CBR and VBR Traffic Workloads”,
   Argyriou, A.; Madisetti, V. K.;

49. “Electronic System, Platform & Package Codesign”,
   Madisetti, V. K.

   A. Argyriou, Madisetti, V. K.

   A. Argyriou, Madisetti, V. K.
52. “Computationally Efficient SNR Estimation for Bandlimited WCDMA Systems”
L. Jatunov, Madisetti, V. K.
IEEE Transactions on Wireless Communications, Volume 5, Issue 13,
December 2006, Pages 3480-3491.

53. “Space-Time Codes for Wireless & Mobile Applications”,
M. Sinnokrot, Madisetti, V.K.


Peer Reviewed Conference Publications

1. **Dynamically-reduced complexity implementation of echo cancelers**  
   Madisetti, V.; Messerschmitt, D.; Nordstrom, N.;  
   Acoustics, Speech, and Signal Processing, IEEE International Conference on  
   ICASSP '86, Volume: 11, Apr 1986

2. **Seismic migration algorithms using the FFT approach on the NCUBE multiprocessor**  
   Madisetti, V.K.; Messerschmitt, D.G.;  
   International Conference on, 11-14 April 1988

3. **Seismic migration algorithms on multiprocessors**  
   Madisetti, V.K.; Messerschmitt, D.G.;  
   International Conference on, 11-14 April 1988
   Pages:2124 - 2127 vol.4

4. **WOLF: A rollback algorithm for optimistic distributed simulation systems**  
   Madisetti, V.; Walrand, J.; Messerschmitt, D.;  
   Pages:296 – 305

5. **Efficient distributed simulation**  
   Madisetti, V.; Walrand, J.; Messerschmitt, D.;  
   Pages:5 - 6

6. **High speed migration of multidimensional seismic data**  
   Kelley, B.; Madisetti, V.;  
   International Conference on, 14-17 April 1991
   Pages:1117 - 1120 vol.2

7. **Performance of a fast analog VLSI implementation of the DFT**  
   Buchanan, B.; Madisetti, V.; Brooke, M.;  
   Circuits and Systems, 1992., Proceedings of the 35th Midwest Symposium on  
   , 9-12 Aug. 1992
   Pages:1353 - 1356 vol.2
8. Task scheduling in the Georgia Tech digital signal multiprocessor
   Curtis, B.A.; Madisetti, V.K.;
   International Conference on ,Volume: 5 , 23-26 March 1992
   Pages:589 - 592 vol.5

9. The fast discrete Radon transform
   Kelley, B.T.; Madisetti, V.K.;
   International Conference on ,Volume: 3 , 23-26 March 1992
   Pages:409 - 412 vol.3

10. Yield-based system partitioning strategies for MCM and ASEM design
    Khan, S.; Madisetti, V.;
    17 March 1994
    Pages:144 – 149

11. Multitrack RLL codes for the storage channel with immunity to
    intertrack interference
    Lee, J.; Madisetti, V.K.;
    Pages:1477 - 1481 vol.3

12. A parallel mapping of backpropagation algorithm for mesh signal
    processor
    Khan, S.A.; Madisetti, V.K.;
    IEEE Workshop , 31 Aug.-2 Sept. 1995
    Pages:561 – 570

13. Virtual prototyping of embedded DSP systems
    International Conference on ,Volume: 4 , 9-12 May 1995
    Pages:2711 - 2714 vol.4

14. Assessing and improving current practice in the design of
    application-specific signal processors
    Shaw, G.A.; Anderson, J.C.; Madisetti, V.K.;
    International Conference on ,Volume: 4 , 9-12 May 1995
    Pages:2707 - 2710 vol.4
15. Introduction to ARPA’s RASSP initiative and education/facilitation program
Corley, J.H.; Madisetti, V.K.; Richards, M.A.;
International Conference on, Volume: 4, 9-12 May 1995
Pages: 2695 - 2698 vol.4

16. DSP design education at Georgia Tech
Madisetti, V.K.; McClellan, J.H.; Barnwell, T.P., III;
International Conference on, Volume: 5, 9-12 May 1995
Pages: 2869 - 2872 vol.5

17. Rapid prototyping of DSP systems via system interface module generation
Famorzadeh, S.; Madisetti, V.K.;
Pages: 1256 - 1259 vol. 2

18. Rapid prototyping of DSP chip-sets via functional reuse
Romdhane, M.S.B.; Madisetti, V.K.;
Pages: 1236 - 1239 vol. 2

19. A constructive deconvolution procedure of bandpass signals by homomorphic analysis
Marenco, A.L.; Madisetti, V.K.;
Pages: 1592 - 1596 vol.3

20. BEEHIVE: an adaptive, distributed, embedded signal processing environment
Famorzadeh, S.; Madisetti, V.; Egolf, T.; Nguyen, T.;
Pages: 663 - 666 vol.1

21. Target detection from coregistered visual-thermal-range images
Perez-Jacome, J.E.; Madisetti, V.K.;
22. Variable block size adaptive lapped transform-based image coding
   Klausutis, T.J.; Madisetti, V.K.;
   Pages: 686 - 689 vol.3

23. A Rate 8/10 (0, 6) MTR Code And Its Encoder/decoder
   Jaejin Lee; Madisetti, V.K.;
   International , 1-4 April 1997
   Pages: BS-15 - BS-15

24. VHDL models supporting a system-level design process: a RASSP approach
   DeBardelaben, J.A.; Madisetti, V.K.; Gadjient, A.J.;
   Pages: 183 – 188

25. A performance modeling framework applied to real time infrared search and track processing
   Pauer, E.K.; Pettigrew, M.N.; Myers, C.S.; Madisetti, V.K.;
   Pages: 33 – 42

26. System design and re-engineering through virtual prototyping: a temporal model-based approach
   Khan, M.H.; Madisetti, V.K.;
   Pages: 1720 - 1724 vol.2

27. A debugger RTOS for embedded systems
   Akgul, T.; Kuacharoen, P.; Mooney, V.J.; Madisetti, V.K.;
   Pages: 264 - 269

28. Adaptability, extensibility and flexibility in real-time operating systems
   Kuacharoen, P.; Akgul, T.; Mooney, V.J.; Madisetti, V.K.;
   Pages: 400 – 405
29. **Effect of handoff delay on the system performance of TDMA cellular systems**  
*Turkboylari, M.; Madisetti, V.K.*;  
Pages: 411 – 415

30. **Enforcing interdependencies and executing transactions atomically over autonomous mobile data stores using SyD link technology**  
*Prasad, S.K.; Bourgeois, A.G.; Dogdu, E.; Sunderraman, R.; Yi Pan; Navathe, S.; Madisetti, V.*;  
Pages: 803 – 809

31. **Performance evaluation and optimization of SCTP in wireless ad-hoc networks**  
*Argyriou, A.; Madisetti, V.*;  
Pages: 317 - 318

32. **Implementation of a calendar application based on SyD coordination links**  
*Prasad, S.K.; Bourgeois, A.G.; Dogdu, E.; Sunderraman, R.; Yi Pan; Navathe, S.; Madisetti, V.*;  
Pages: 8 pp.

33. **Bandwidth aggregation with SCTP**  
*Argyriou, A.; Madisetti, V.*;  
Pages: 3716 - 3721 vol.7

34. **Software streaming via block streaming**  
*Kuacharoen, P.; Mooney, V.J.; Madisetti, V.K.*;  
Pages: 912 – 917

35. **Frequency-dependent space-interleaving for MIMO OFDM systems**  
*Mohajerani, P.; Madisetti, V.K.*;  
Radio and Wireless Conference, 2003. RAWCON '03. Proceedings, Aug. 10-
36. A media streaming protocol for heterogeneous wireless networks
Argyriou, A.; Madisetti, V.;
Pages: 30 – 33

37. Realizing load-balancing in ad-hoc networks with a transport layer protocol
Argyriou, A.; Madisetti, V.;
Pages: 1897 - 1902 Vol.3

38. Streaming H.264/AVC video over the Internet
Argyriou, A.; Madisetti, V.;
Pages: 169 – 174

Other Publications

   Madisetti, V., Argyriou, A.

2. Voice & Video over Mobile IP Networks <draft-madisetti-argyriou-voice-video-mip-00.txt>
   Madisetti, V., Argyriou, A.

3. Enhancements to ECRTP with Applications to Robust Header Compression for Wireless Applications. <draft-madisetti-rao-suresh-rohc-00.txt>
   Madisetti, V.; Rao, S., Suresh, N.
Ph.D. Students Graduated

1. Brian T. Kelley, 1992
   VLSI Computing Architectures for High Speed Signal Processing
   Member of Technical Staff, Motorola.

   Winner of Dr. Thurgood Marshall Dissertation Fellowship Award

2. Bryce A. Curtis, 1992
   Special Instruction Set Multiple Chip Computer for DSP
   Member of Technical Staff, IBM

   Robust Multitrack Codes for the Magnetic Channel
   Professor, Yonsei University, Korea

4. Mohamed S. Ben Romdhane, 1995
   Design Synthesis of Application-Specific IC for DSP
   Director of IP, Rockwell.

5. Shoab A. Khan, 1995
   Logic and Algorithm Partitioning on MCMs
   Professor, National University of Science & Technology, Pakistan

   VHDL-based Conceptual Prototyping of Embedded DSP Architectures
   Professor, National Chaio Tung University, Taiwan.

   Winner of VHDL International Best PhD Thesis Award, 1997

7. Thomas W. Egolf, 1997
   Virtual Prototyping of Embedded DSP Systems
   Distinguished Member of Technical Staff, Agere

8. Alvaro Marenco, 1997
   On Homomorphic Deconvolution of Bandpass Signals
   Professor, Texas A&M University.

   Winner of GIT ECE Outstanding Teaching Assistant Award

Professor Vijay K. Madisetti, ECE

BEEHIVE: A Distributed Environment for Adaptive Signal Processing
Member of Technical Staff, Rockwell.

10. Timothy J. Klausutis, 1997
   Adaptive Lapped Transforms with Applications to Image Coding.

11. Lan Shen, 1998
   Temporal Design of Core-Based Systems
   Member of Technical Staff, IBM

   Optimization Based Approach to Cost Effective DSP Design
   Research Scientist, Johns Hopkins University

   Georgia Tech ECE Faculty Award

13. Sangyoun Lee, 1999
   Design of Robust Video Signal Processors
   Professor, Yonsei University

   US Army Sensors Lab Research Excellence Award, 1999

   Oversampled Digital Filters
   Member of Technical Staff, Texas Instruments

15. Yong-kyu Jung, 2001
   Model-Based Processor Synthesis
   Professor, Texas A&M University

16. Mustafa Turkboyliari, 2002
   Handoff Algorithms for Wireless Applications
   Member of Technical Staff, Texas Instruments

17. Yun-Hui Fan, 2002
   A Stereo Audio Coder with Nearly Constant Signal to Noise Ratio
   Post-Doctoral Research Associate, Northeastern University

18. Subrato K. De, 2002
   Design of a Retargetable Compiler for DSP
   Member of Technical Staff, Qualcomm

   US Army Sensors Lab Research Excellence Award, 1999

19. Chonlameth Arinikanondt, 2004
   System-on-Chip Design with UML
   Professor, King Mongkut’s University, Thailand.

   US Army Sensors Lab Research Excellence Award, 1999

20. Loran Jatunov, 2004
   Performance Analysis of 3G CDMA Systems
Professor Vijay K. Madisetti, ECE

Senior Research Scientist, Soft Networks, LLC.


22. **Pilho Kim**, 2009, **Scientist, VP Technologies, Inc.**

23. **M. Sinnokrot**, 2009, **Staff Engineer, Qualcomm.**

---

**Awards & Honors**


3. **Demetri Angelakos Outstanding Graduate Student Award**, Univ. of California, Berkeley, 1989


5. **IBM Faculty Development Award** 1990


7. **Technical Program Chair**, IEEE MASCOTS’94

8. **NSF RI Award**, 1990

9. **VHDL International Best PhD Dissertation Advisor Award**, 1997


12. **Fellow of IEEE**
### Intellectual Property Disclosures (Georgia Tech)

<table>
<thead>
<tr>
<th>Patent</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2843</td>
<td>2004</td>
<td>Method and Apparatus for Improving the Performance of Wireless LANs</td>
</tr>
<tr>
<td>2825</td>
<td>2003</td>
<td>Method and Apparatus for Optimal Partitioning and Ordering of Antennas for</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Layered Space-Time Block Codes in MIMO Communications Systems</td>
</tr>
<tr>
<td>2815</td>
<td>2003</td>
<td>How to Rapidly Develop a SyD Application</td>
</tr>
<tr>
<td>GSU-023</td>
<td>2003</td>
<td>Rapid Development of SyD Applications</td>
</tr>
<tr>
<td>2810</td>
<td>2003</td>
<td>System on Mobile Devices Middleware Design</td>
</tr>
<tr>
<td>2718</td>
<td>2003</td>
<td>A Transport Layer Algorithm for Improved Anycast Communication</td>
</tr>
<tr>
<td>2717</td>
<td>2003</td>
<td>A Novel Transport Layer Load-Balancing Algorithm</td>
</tr>
<tr>
<td>2716</td>
<td>2003</td>
<td>A Transport Layer QoS Algorithm</td>
</tr>
<tr>
<td>2715</td>
<td>2003</td>
<td>A Novel Transport Layer Algorithm for MPLS Performance</td>
</tr>
<tr>
<td>2659</td>
<td>2002</td>
<td>A New Algorithm and Technology for Implementing Mobile IP with Applications</td>
</tr>
<tr>
<td></td>
<td></td>
<td>to Voice and Video over Mobile IP</td>
</tr>
<tr>
<td>2656</td>
<td>2002</td>
<td>Debugging with Instruction-Level Reverse Execution</td>
</tr>
<tr>
<td>2655</td>
<td>2002</td>
<td>Embedded Software Streaming</td>
</tr>
<tr>
<td>Year</td>
<td>Title</td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>----------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>2002</td>
<td>A Dynamic Instantiated Real-Time Operating System Debugger</td>
<td></td>
</tr>
<tr>
<td>2002</td>
<td>A Dynamic Real-Time Operating System</td>
<td></td>
</tr>
<tr>
<td>2001</td>
<td>System of Databases: Architecture, Global Queries, Triggers and Constraints</td>
<td></td>
</tr>
<tr>
<td>2001</td>
<td>Mobile Fleet Application based on SyD Technology</td>
<td></td>
</tr>
<tr>
<td>2001</td>
<td>System of Databases: A model with coordination links and a calendar application</td>
<td></td>
</tr>
<tr>
<td>1999</td>
<td>Beehive</td>
<td></td>
</tr>
<tr>
<td>1995</td>
<td>Very High Scale Integrated Circuit Hardware Description Language Models (VHDL Models)</td>
<td></td>
</tr>
<tr>
<td>1995</td>
<td>Self-Compensation Receiver (SCR)</td>
<td></td>
</tr>
</tbody>
</table>
Appendix B
Materials Considered

- U.S. Patent No. 6,611,247
- File history of U.S. Patent No. 6,611,247
- U.S. Patent No. 6,320,590 to Yong-Suk Go
- U.S. Patent No. 5,913,075 to Beers et al.
- U.S. Patent No. 5,900,857 to Kuwata et al.
- U.S. Patent No. 6,324,602 to Chen et al.
- U.S. Patent No. 5,793,223 to Richard F. Frankeney